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REVA UNIVERSITY
Bengaluru, India

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

M. TECH IN VLSI & EMBEDDED SYSTEMS-FT

HAND BOOK: 2021-23

Rukmini Educational
Charitable Trust

OUR VISION

REVA University aspires to become an innovative university by developing excellent human resources with leadership qualities, ethical and moral values, research culture and innovative skills through higher education of global standards.

OUR MISSION

1. To create excellent infrastructure facilities and state- of- the -art laboratories and incubation centers .
2. To provide student-centric learning environment through innovative pedagogy and educational reforms.
3. To encourage research and entrepreneurship through collaborations and extension activities.
4. To promote industry-institute partnerships and share knowledge for innovation and development.
5. To organize social development programs for knowledge enhancement in thrust areas.
6. To enhance leadership qualities among youth, to enrich personality traits and promote patriotism and moral values;

BROAD OBJECTIVES

1. Creation, preservation and dissemination of knowledge and attainment of excellence in different disciplines.
2. Smooth transition from teacher - centric focus to learner - centric processes and activities.
3. Performing all the functions of interest to its major constituents like faculty, staff, students and society to reach leadership positions.
4. Developing a sense of ethics in the University community, making it conscious of its obligations to society and the nation.
5. Accepting the challenges of globalization to offer high quality education and other services in a competitive manner.

DO'S AND DON'TS

DO'S

1. Maintain discipline and respect the rules and regulations of the university
2. Be regular and punctual to classes
3. Study regularly and submit assignments on time
4. Be respectful to your Teaches/friends and hostel staff/management.
5. Read the notice board (both at your college and the hostel) regularly.
6. Utilize your Personal Computer for educational purpose only.
7. Follow the code of conduct.
8. Visit Health Center on the campus whenever you are unwell.
9. Be security conscious and take care of your valuables especially Cash, Mobile Phones, Laptop andother valuables.
10. Carry your valuables along with you whenever you proceed on leave/vacation.
11. Use electric appliances, lights and water optimally.
12. Keep the campus clean and hygienic.
13. Use decent dressing.

DON'TS

1. Ragging inside / outside the campus.
2. Possession of Fire arms and daggers etc.
3. Use of Alcohols, Toxic drugs, sheesha, gutkha and hashish/heroin etc.
4. Use of Crackers, explosives and ammUNIT - ion etc.
5. Smoking and keeping any kind of such items.
6. Misusing college & hostel premises/facilities for activities other than studies.
7. Playing loud music in the room which may disturb studies of colleagues / neighbours.
8. Making noise and raising slogans.
9. Keeping electrical appliances, other than authorized ones.
10. Involvement in politics, ethnic, sectarian and other undesirable activities.
11. Proxy in any manner.
12. Use of mobiles in the academic areas.

Note: 1. Rules are revised / reviewed as and when required.
2. Healthy suggestions are welcome for betterment of Institution

REVA UNIVERSITY
Bengaluru, India

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

HANDBOOK

M. Tech. in VLSI and Embedded Systems (FT)

2021-23

Rukmini Knowledge Park,
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Phone No: +91-080-66226622, Fax: 080-28478539

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Chancellor's Message

"Education is the most powerful weapon which you can use to change the world."
- Nelson Mandela.

There was a time when survival depended on just the realization of physiological needs. We are indeed privileged to exist in a time when 'intellectual gratification' has become indispensable. Information is easily attainable for the soul that is curious enough to go look for it. Technological boons enable information availability anywhere anytime. The difference, however, lies between those who look for information and those who look for knowledge.

It is deemed virtuous to serve seekers of knowledge and as educators it is in the ethos at REVA University to empower every learner who chooses to enter our portals. Driven by our founding philosophy of 'Knowledge is power', we believe in building a community of perpetual learners by enabling them to look beyond their abilities and achieve what they assumed impossible.

India has always been beheld as a brewing pot of unbelievable talent, acute intellect and immense potential. All it takes to turn those qualities into power is a spark of opportunity. Being at a University is an exciting and rewarding experience with opportunities to nurture abilities, challenge cognizance and gain competence.

For any University, the structure of excellence lies in the transitional abilities of its faculty and its facility. I'm always in awe of the efforts that our academic board puts in to develop the team of subject matter experts at REVA. My faculty colleagues understand our core vision of empowering our future generation to be ethically, morally and intellectually elite. They practice the art of teaching with a student-centered and transformational approach. The excellent infrastructure at the University, both educational and extra-curricular, magnificently demonstrates the importance of ambience in facilitating focused learning for our students.

A famous British politician and author from the 19th century - Benjamin Disraeli, once said 'A University should be a place of light, of liberty and of learning'. Centuries later this dictum still inspires me and I believe, it takes team-work to build successful institutions. I welcome you to REVA University to join hands in laying the foundation of your future with values, wisdom and knowledge.

Dr. P. Shyama Raju
The Founder and Hon'ble Chancellor, REVA University

Vice-Chancellor's Message

The last two decades have seen a remarkable growth in higher education in India and across the globe. The move towards inter-disciplinary studies and interactive learning have opened up several options as well as created multiple challenges. A strong believer and practitioner of the dictum "Knowledge is Power", REVA University has been on the path of delivering quality education by developing the young human resources on the foundation of ethical and moral values, while boosting their leadership qualities, research culture and innovative skills. Built on a sprawling 45 acres of green campus, this 'temple of learning' has excellent and state-of-the-art infrastructure facilities conducive to higher teaching-learning environment and research. The main objective of the University is to provide higher education of global standards and hence, all the programs are designed to meet international standards. Highly experienced and qualified faculty members, continuously engaged in the maintenance and enhancement of student-centric learning environment through innovative pedagogy, form the backbone of the University.

All the programs offered by REVA University follow the Choice Based Credit System (CBCS) with Outcome Based Approach. The flexibility in the curriculum has been designed with industry-specific goals in mind and the educator enjoys complete freedom to appropriate the syllabus by incorporating the latest knowledge and stimulating the creative minds of the students. Bench marked with the course of studies of various institutions of repute, our curriculum is extremely contemporary and is a culmination of efforts of great think-tanks - a large number of faculty members, experts from industries and research level organizations. The evaluation mechanism employs continuous assessment with grade point averages. We believe sincerely that it will meet the aspirations of all stakeholders – students, parents and the employers of the graduates and postgraduates of Reva University.

At REVA University, research, consultancy and innovation are regarded as our pillars of success. Most of the faculty members of the University are involved in research by attracting funded projects from various research level organizations like DST, VGST, DBT, DRDO, AICTE and industries. The outcome of the research is passed on to students through live projects from industries. The entrepreneurial zeal of the students is encouraged and nurtured through EDPs and EACs.

With firm faith in the saying, "Intelligence plus character –that is the goal of education" (Martin Luther King, Jr.), I strongly believe REVA University is marching ahead in the right direction, providing a holistic education to the future generation and playing a positive role in nation building. We reiterate our endeavor to provide premium quality education accessible to all and an environment for the growth of over-all personality development leading to generating "GLOBAL PROFESSIONALS".

Welcome to the portals of REVA University!

Director's –Message

Since the inception of REVA University, School of Electronics and Communication Engineering is involved in implementing following best practices in various dimensions such asacademics, research, outreach activities, student development programs, project based and research based learning, student centric learning, student competitions, industry and in-house internships, abroad internships, skill enhancement activities, motivation for competitive exams, mini projects, major projects, industry mentored projects, multidisciplinary projects, industry visits, technical talks by industry and academicians, certification programs, etc.Individual students are taken care by strong mentoring system wherein faculty members are not only allotted as mentorsto students, but also they will act as local guardians and they will have constant follow up with mentees in regard to academic and personal issues till students complete the degree.

The curriculum is carefully designed to meet the current industry trends and also to provide insight into future technology developments that lead to inculcate lifelong learning abilities in students. Board of Studies (BoS) comprises people from academics, industry, alumni and current students which form the strong backbone for our programs wherein constant updates happen in contents/subjects every semester based on current industry needs. Curriculum has good mix of foundation courses, hardcore courses, softcore courses, practicals and projects along with open electives, softskill and skill development courses.

Student's welfare is given utmost priority at School of Electronics and Communication Engineering. Advanced learning methods are adopted to make learning truly interactive. More focus is on discussion and practical applications rather than rote learning. Notes/handouts/video contents/quizzes are given and critical thinking questions are asked to test understanding. Experienced, well qualified and friendly faculty members always strive hard to provide best of education to students. The faculty members have number of publications in reputed national and international journals/conferences. The school is also involved in funded research projects.

I am sure the students choosing B Tech and M. Tech programs in School of Electronics and Communication Engineering in REVA University will enjoy the curriculum, teaching and learning environment, well equipped laboratories, digital classrooms infrastructure and the experienced teachers involvement and guidance. The curriculum caters to and has relevance to local, regional, national, global, developmental need. Maximum number of courses are integrated with cross cutting issues with relevant to professional Ethics, Gender, Human values, Environment, and Sustainability.

RUKMINI EDUCATIONAL CHARITABLE TRUST

It was the dream of late Smt. Rukmini Shyama Raju to impart education to millions of underprivileged children as she knew the importance of education in the contemporary society. The dream of Smt. Rukmini Shyama Raju came true with the establishment of Rukmini Educational Charitable Trust (RECT), in the year 2002. **Rukmini Educational Charitable Trust** (RECT) is a Public Charitable Trust, set up in 2002 with the objective of promoting, establishing and conducting academic activities in the fields of Arts, Architecture, Commerce, Education, Engineering, Environmental Science, Legal Studies, Management and Science & Technology, among others. In furtherance of these objectives, the Trust has set up the REVA Group of Educational Institutions comprising of REVA Institute of Technology & Management (RITM), REVA Institute of Science and Management (RISM), REVA Institute of Management Studies (RIMS), REVA Institute of Education (RIE), REVA First Grade College (RFGC), REVA Independent PU College at Kattigenahalli, Ganganagar and Sanjaynagar and now REVA University. Through these institutions, the Trust seeks to fulfill its vision of providing world class education and create abundant opportunities for the youth of this nation to excel in the areas of Arts, Architecture, Commerce, Education, Engineering, Environmental Science, Legal Studies, Management and Science & Technology.

Every great human enterprise is powered by the vision of one or more extraordinary individuals and is sustained by the people who derive their motivation from the founders. The Chairman of the Trust is Dr. P. Shyama Raju, a developer and builder of repute, a captain of the industry in his own right and the Chairman and Managing Director of the DivyaSree Group of companies. The idea of creating these top notched educational institutions was born of the philanthropic instincts of Dr. P. Shyama Raju to do public good, quite in keeping with his support to other socially relevant charities such as maintaining the Richmond road park, building and donating a police station, gifting assets to organizations providing accident and trauma care, to name a few.

The Rukmini Educational Charitable Trust drives with the main aim to help students who are in pursuit of quality education for life. REVA is today a family of ten institutions providing education from PU to Post Graduation and Research leading to PhD degrees. REVA has well qualified experienced teaching faculty of whom majority are doctorates. The faculty is supported by committed administrative and technical staff. Over 13,000 students study various courses across REVA's three campuses equipped with exemplary state-of-the-art infrastructure and conducive environment for the knowledge driven community.

ABOUT REVA UNIVERSITY

REVA University has been established under the REVA University Act, 2012 of Government of Karnataka and notified in Karnataka State Gazette No. 80 dated 27thFebruary, 2013. The University is empowered by UGC to award degrees any branch of knowledge under Sec.22 of the UGC Act. The University is a Member of Association of Indian Universities, New Delhi. The main objective of the University is to prepare students with knowledge, wisdom and patriotism to face the global challenges and become the top leaders of the country and the globe in different fields.

REVA University located in between Kempegowda International Airport and Bangalore city, has a sprawling green campus spread over 45 acres of land and equipped with state-of-the-art infrastructure that provide conducive environment for higher learning and research. The REVA campus has well equipped laboratories, custom-built teaching facilities, fully air-conditioned library and central computer centre, the well planned sports facility with cricket ground, running track & variety of indoor and outdoor sports activities, facilities for cultural programs. The unique feature of REVA campus is the largest residential facility for students, faculty members and supportive staff.

REVA consistently ranked as one of the top universities in various categories because of the diverse community of international students and its teaching excellence in both theoretical and technical education in the fields of Engineering, Management, Law, Science, Commerce, Arts, Performing Arts, and Research Studies. REVA offers 28 Undergraduate Programmes, 22 Full-time and 2 Part-time Postgraduate Programmes, 18 Ph. D Programmes, and other Certificate/ Diploma/Postgraduate Diploma Programmes in various disciplines.

The curriculum of each programme is designed with a keen eye for detail by giving emphasis on hands-on training, industry relevance, social significance, and practical applications. The University offers world-class facilities and education that meets global standards.

The programs being offered by the REVA University are well planned and designed after detailed study with emphasis with knowledge assimilation, applications, global job market and their social relevance. Highly qualified, experienced faculty and scholars from reputed universities / institutions, experts from industries and business sectors have contributed in preparing the scheme of instruction and detailed curricula for this program. Greater emphasis on practice in respective areas and skill development to suit to respective job environment has been given while designing the curricula. The Choice Based Credit System and Continuous Assessment Graded Pattern (CBCS – CAGP) of education

has been introduced in all programs to facilitate students to opt for subjects of their choice in addition to the core subjects of the study and prepare them with needed skills. The system also allows students to move forward under the fast track for those who have the capabilities to surpass others. These programs are taught by well experienced qualified faculty supported by the experts from industries, business sectors and such other organizations. REVA University has also initiated many supportive measures such as bridge courses, special coaching, remedial classes, etc., for slow learners so as to give them the needed input and build in them confidence and courage to move forward and accomplish success in their career. The University has also entered into MOUs with many industries, business firms and other institutions seeking their help in imparting quality education through practice, internship and also assisting students' placements.

REVA University recognizing the fact that research, development and innovation are the important functions of any university has established an independent Research and Innovation division headed by a senior professor as Dean of Research and Innovation. This division facilitates all faculty members and research scholars to undertake innovative research projects in engineering, science & technology and other areas of study. The interdisciplinary-multidisciplinary research is given the top most priority. The division continuously liaisons between various funding agencies, R&D Institutions, Industries and faculty members of REVA University to facilitate undertaking innovative projects. It encourages student research projects by forming different research groups under the guidance of senior faculty members. Some of the core areas of research wherein our young faculty members are working include Data Mining, Cloud Computing, Image Processing, Network Security, VLSI and Embedded Systems, Wireless Censor Networks, Computer Networks, IOT, MEMS, Nano- Electronics, Wireless Communications, Bio-fuels, Nano-technology for coatings, Composites, Vibration Energies, Electric Vehicles, Multilevel Inverter Application, Battery Management System, LED Lightings, Renewable Energy Sources and Active Filter, Innovative Concrete Reinforcement, Electro Chemical Synthesis, Energy Conversion Devices, Nano-structural Materials, Photo-electrochemical Hydrogen generation, Pesticide Residue Analysis, Nano materials, Photonics, Nana Tribology, Fuel Mechanics, Operation Research, Graph theory, Strategic Leadership and Innovative Entrepreneurship, Functional Development Management, Resource Management and Sustainable Development, Cyber Security, General Studies, Feminism, Computer Assisted Language Teaching, Culture Studies etc.

The REVA University has also given utmost importance to develop the much required skills through variety of training programs, industrial practice, case studies and such other activities that induce the said skills among all students. A full-fledged Career Development and Placement (CDC) department with world class infrastructure, headed by a dynamic experienced Professor& Dean, and supported by

well experienced Trainers, Counselors and Placement Officers.

The University also has University-Industry Interaction and Skill Development Centre headed by a Senior Professor & Director facilitating skill related training to REVA students and other unemployed students. The University has been recognised as a Centre of Skill Development and Training by NSDC (National Skill Development Corporation) under Pradhan Mantri Kaushal VikasYojana. The Centre conducts several add-on courses in challenging areas of development. It is always active in facilitating student's variety of Skill Development Training programs.

The University has collaborations with Industries, universities abroad, research institutions, corporate training organizations, and Government agencies such as Florida International University, Okalahoma State University, Western Connecticut University, University of Alabama, Huntsville, Oracle India Ltd, Texas Instruments, Nokia University Relations, EMC^2, VMware, SAP, Apollo etc, to facilitate student exchange and teacher–scholar exchange programs and conduct training programs. These collaborations with foreign universities also facilitates students to study some of the programs partly in REVA University and partly in foreign university, viz, M.S in Computer Science one year in REVA University and the next year in the University of Alabama, Huntsville, USA.

The University has also given greater importance to quality in education, research, administration and all activities of the university. Therefore, it has established an independent Internal Quality division headed by a senior professor as Dean of Internal Quality. The division works on planning, designing and developing different quality tools, implementing them and monitoring the implementation of these quality tools. It concentrates on training entire faculty to adopt the new tools and implement their use. The division further works on introducing various examination and administrative reforms.

To motivate the youth and transform them to become innovative entrepreneurs, successful leaders of tomorrow and committed citizens of the country, REVA organizes interaction between students and successful industrialists, entrepreneurs, scientists and such others from time to time. As a part of this exercise great personalities such as Bharat Ratna Prof. C. N. R. Rao, a renowned Scientist, Dr. N R Narayana Murthy, Founder and Chairman and Mentor of Infosys, Dr. K Kasturirangan, Former Chairman ISRO, Member of Planning Commission, Government of India, Dr. Balaram, Former Director IISc., and noted Scientist, Dr. V S Ramamurthy, Former Secretary, DST, Government of India, Dr. V K Aatre, noted Scientist and former head of the DRDO and Scientific Advisor to the Ministry of Defence Dr. Sathish Reddy, Scientific Advisor, Ministry of Defence, New Delhi and many others have accepted

our invitation and blessed our students and faculty members by their inspiring addresses and interaction.

REVA organises various cultural programs to promote culture, tradition, ethical and moral values to our students. During such cultural events the students are given opportunities to unfold their hidden talents and motivate them to contribute innovative ideas for the progress of the society. One of such cultural events is REVAMP conducted every year. The event not only gives opportunities to students of REVA but also students of other Universities and Colleges. During three days of this mega event students participate in debates, Quizzes, Group discussion, Seminars, exhibitions and variety of cultural events. Another important event is Shubha Vidaaya, - Graduation Day for the final year students of all the programs, wherein, the outgoing students are felicitated and are addressed by eminent personalities to take their future career in a right spirit, to be the good citizens and dedicate themselves to serve the society and make a mark in their respective spheres of activities. During this occasion, the students who have achieved top ranks and won medals and prizes in academic, cultural and sports activities are also recognised by distributing awards and prizes. The founders have also instituted medals and prizes for sports achievers every year. The physical education department conducts regular yoga class'severyday to students, faculty members, administrative staff and their family members and organizes yoga camps for villagers around.

Vision

REVA University aspires to become an innovative university by developing excellent human resources with leadership qualities, ethical and moral values, research culture and innovative skills through higher education of global standards.

Misson

- To create excellent infrastructure facilities and state-of-the-art laboratories and incubation centers
- To provide student-centric learning environment through innovative pedagogy and education reforms
- To encourage research and entrepreneurship through collaborations and extension activities
- To promote industry-institute partnerships and share knowledge for innovation and development
- To organize society development programs for knowledge enhancement in thrust areas
- To enhance leadership qualities among the youth and enrich personality traits, promote patriotism and moral values.

Objectives

- Creation, preservation and dissemination of knowledge and attainment of excellence in different disciplines
- Smooth transition from teacher - centric focus to learner - centric processes and activities
- Performing all the functions of interest to its major constituents like faculty, staff, students and the society to reach leadership position
- Developing a sense of ethics in the University and Community, making it conscious of its obligations to the society and the nation
- Accepting the challenges of globalization to offer high quality education and other services in a competitive manner

ABOUT SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

The School of Electronics and Communication Engineering headed by a highly experienced Professor and is supported by well qualified faculty members. The school has the state-of-art class rooms and well equipped laboratories. It offers B.Tech and M.Techand PhD programs in various specialized streams. The curriculums of both the graduate and the post graduate degree programs have been designed to meet the current industry trends. B. Tech program aims to prepare human resources to play a leading role in the continuing adventure of modern automated systems and communications. The program offers numerous choices of study for the students based on interest in the current state of art technology. Apart from fundamental courses in Electronics and Communication Engineering, the school facilitates to study in four streams such as Circuits and Devices, Communication Engineering, Signal Processing and Programming. Students are at liberty to choose from these streams in higher semesters. This is reflected in various core subjects offered within the program.

The Master degree programs focus on research and design in the core and IT industries, building and marketing the next generation of product development. These programs provide an opportunity to explore newer dimensions in cutting edge tecghnologies like VLSI, Embedded Systems, Communication and Networking and pursue research in interested domains for doctoral degree.

Vision

The School of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering blended by research and innovation in tune with changing technological and cultural challenges supported with leadership qualities, ethical and moral values.

Mission

- Establish a unique learning environment to enable the students to face the challenges in the field of Electronics and Communication Engineering and explore multidisciplinary which serve the socetial requirements.
- Create state-of-the-art labrotaries, resources and exposure to the current industrial trends to enable students to develop skills for solving complex technological problems of current times and also provide a framework for promoting collaborative and multidisciplinary activities.
- Promote the establishment of Centers of Excellence in niche technology areas to nurture the spirit of innovation and creativity among faculty and students.

- Offer ethical and moral value based education by promoting activities which inculcate the leadership qualities, patriotism and set high benchmarks to serve the society.

Program Overview

Electronics and Communication Engineering is an engineering discipline involved design, development, manufacture and deployment of Electronic and Communication systems. It deals with electronic devices, circuits, communication equipment like transmitter, receiver, integrated circuits (IC), analog and digital transmission and reception of data, voice and video, microprocessors, satellite communication, microwave engineering, antennae and wave progression. Signal and Image processing, Communication Technologies, Embedded Systems, VLSI Systems are some of the specialized areas available in electronics for further study.

Very Large Scale Integration (VLSI) system design is the process of creating complex integrated circuits by combining million/billion number of transistors into a single chip. This programme aims to prepare the students to design analog and digital integrated circuits using custom and semicustom design flow.Worldwide, for the past five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The improvement of integration level, cost, speed, power, compactness and functionality of the integrated circuits leads to significant improvement in economic productivity and overall quality of life through proliferation of computers, communication, industrial and consumer electronics.The improvement and complexity of VLSI system can be achieved by revolution of CMOS transistors, miniaturization of transistors, VLSI design methodology, EDA tool support, fabrication support, new design idea and innovative technology which are active research area in VLSI system design.

The ICs/Micro Processor/Micro-Controller/ chips developed and fabricated using VLSI technology become the heart of embedded systems. Embedded systems have become pervasive across various domains such as automotive, industrial and communication systems leading to tremendous growth in the application and innovation of networked and high performance real time embedded systems.To sustain the growth rate, the organizations involved in VLSI technology and Embedded Systems development are in need of designers, analysts, developers, manufacturing, testing and marketing engineers as well as managers with a postgraduate degree in VLSI design and Embedded System sector.

The School of Electronics and Communication Engineering at REVA UNIVERSITY offers M. Tech., in VLSI and Embedded Systems–a postgraduateprogramme to create motivated, innovative, creative and thinking graduates to fill the roles of Electronic Engineers who can conceptualize, design, analyze and develop VLSI and Embedded systems to meet the modern day requirements.

The number of product and service based semiconductor industry are growing, thus various career opportunities exist in product development companies including mobile and consumer electronics, computing, telecommunications, networking, data processing, automotive, healthcare and industrial applications.
In this context**,** The School of Electronics and Communication Engineering at REVA UNIVERSITY would like to add to the growing human resources needs of VLSI and embedded system sector as engineers through its M. Tech. programme in VLSI and Embedded Systems.

During the programme the theoretical foundation is built through courses like Digital VLSI design, High speed VLSI design, Low power VLSI Design, Analog and mixed mode design,

system on chip design. The practice includes skill development in both Front end and Back end designs, verification and testing. The program also offers strong knowledge and practical skills in developing embedded solutions on varied platforms such as FPGA, Advanced microcontrollers and processors. The students learn to implement real time embedded systems. The designers gain practical knowledge through mini and major projects in both VLSI and Embedded system design domains.

Program Educational Objectives (PEO's)

The programme educational objectives of the Electronics and Communication Engineering of REVA University is to prepare graduates

PEO-1	To have successful professional careers in national and multinational organization and communicate effectively as a member of a team orto lead a team.
PEO-2	To continue to learn and advance their careers throughactivities such asresearch and development, acquiring doctoral degree, participation in national level research programmes, teaching and research at university level etc.,
PEO-3	To be active members ready to serve the society locally and internationally, may takeupentrpreneurship for the growth of economy and to generate employment; and adopt the philosopy of lifelong learning to be aligned with economic and technological development.

Program Outcomes (POs)

After successful completion of the programme, the graduates shall be able to

PO1. **Demonstrate in-depth knowledge** of VLSI and Embeded Systems, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO2. **Analyze complex engineering problems critically**, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

PO3. **Think laterally and originally, conceptualize and solve engineering problems, evaluate** a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO4. **Extract information pertinent to unfamiliar problems through literature survey and experiments**, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

PO5. **Create, select, learn and apply appropriate techniques**, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

PO6. **Possess knowledge and understanding of group dynamics, recognize** opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO7**. Demonstrate knowledge and understanding** of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors.

PO8. **Communicate with the engineering community, and with society at large**, regarding **complex engineering activities** confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO9: **Recognize the need for**, and have the preparation and ability to engage in **life-long learning** independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10. **Acquire professional and intellectual integrity,** professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11. **Observe and examine critically the outcomes** of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback (**SELF learning**)

Programme Specific Outcomes (PSO's)

After successful completion of the programme, the graduates shall be able to

1. Isolate and solve complex problems in the domains of VLSI and Embedded Systems using latest hardware and software tools and technologies, along with analytical and managerial skills to arrive at cost effective and optimum solutions either independently or as a team.
2. Implant the capacity to apply the concepts of FPGA, ASIC, System On Chip, IoT and cyber physical systems, etc. in the design, development and implementation of application oriented engineering systems
3. Design, Model, Analyze and VLSI and Embedded Systems to solve real life and industry problems.

Regulations – M Tech., Degree Program
Academic Year 2020-21 Batch

(Framed as per the provisions under Section 35 (ii), Section 7 (x) and Section 8 (xvi) & (xxi) of the REVA University Act, 2012)

1. Title and Commencement:

1.1 These Regulations shall be called **"REVA University Academic Regulations – M Tech., Degree Program 2020-21 Batch subject to amendments from time to time by the Academic Council on recommendation of respective Board of Studies and approval of Board of Management**

1.2 These Regulations shall come into force from the date of assent of the Chancellor.

2. The Programs:

These regulations cover the following M Tech., Degree programs of REVA University offered during 2020-21

M Tech (Full Time) in:
Artificial Intelligence
Computer Science and Engineering
Computer Aided Structural Engineering
Construction Technology & Management
Digital Communication and Networking
Machine Design
Power Energy & Systems
Transportation Engineering and Management
VLSI and Embedded Systems

Also
M Tech (Part Time) in:
Computer Science and Engineering
VLSI and Embedded Systems

3. Duration and Medium of Instructions:

3.1 **Duration:** The duration of theM Tech degree program shall be **TWO years** comprising of **FOUR** Semesters. A candidate can avail a maximum of 8 semesters - 4 years as per double duration norm, in one stretch to complete M Tech degree. The duration for part time students is **THREE years** and a maximum of 6 years they are required to complete the program.

3.2 The medium of instruction shall be English.

4. Definitions:

4.1 Course: "Course" means a subject, either theory or practical or both, listed under a programme; Example: "Finite Element Method of Analysis" in M Tech Civil Engineering program, "Advanced Theory of Vibration" in M Tech., Mechanical program are examples of courses to be studied under respective programs.

Every course offered will have three components associated with the teaching-learning process of the course, namely:

L	**Lecture**
T	**Tutorial**
P	**Practice**

Where:

L stands for **Lecture** session consisting of classroom instruction.

T stands for **Tutorial** session consisting participatory discussion / self-study/ desk work/ brief seminar presentations by students and such other novel methods that make a student to absorb and assimilate more effectively the contents delivered in the Lecture classes.

P stands for **Practice** session and it consists of Hands on Experience / Laboratory Experiments / Field Studies / Case Studies / Project Based Learning or Course end Project/Self Study/ Online courses from listed portals that equip students to acquire the much required skill component.

4.2 Classification of Courses

Courses offered are classified as: Core Courses, Open Elective Courses, Project work/Dissertation

4.2.1 **Core Course:** A course which should compulsorily be studied by a candidate choosing a particular program of study

4.2.2 **Foundation Course:** The foundation Course is a mandatory course which should be completed successfully as a part of graduate degree program irrespective of the program of study

4.2.3 **Hard Core Course (HC) simply core course:** The **Hard Core Course** is a Core Course in the main branch of study and related branch(es) of study, if any, that the candidates have to complete compulsorily

4.2.4 **Soft Core Course (SC) (also known as Professional Elective Course)**

A Core course may be a **Soft Core** if there is a choice or an option for the candidate to choose a course from a pool of courses from the main branch of study or from a sister/related branch of study which supports the main branch of study

4.2.5 **Open Elective Course (OE):**

An elective course chosen generally from other discipline / subject, with an intention to seek exposure to the basics of subjects other than the main discipline the student is studying is called an **Open Elective Course**

4.2.6 **Project Work / Dissertation:**

Project work / Dissertation work is a special course involving application of knowledge in solving / analysing /exploring a real life situation / difficult problems to solve a multivariable or complex engineering problems.

5. Eligibility for Admission:

5.1. The eligibility criteria for admission to M Tech Program (Full Time) of 2 years (4 Semesters) and (Part Time) of 3 years (6 Semesters) are given below:

Sl. No.	Program	Duration	Eligibility
1	Masters of Technology (M Tech) in Artificial Intelligence	4 Semesters (2 years)	B E / B.Tech. in CSE / ISE / TE / MCA / M. Sc. in Computer Science or Mathematics or Information Science or Information Technology with a minimum of 50% (45% in case of SC/ST) marks in aggregate of any recognized University / Institution or AMIE or any other qualification recognized as equivalent there to.

2	M Tech in Computer Science and Engineering	**Full Time** – 4 Semesters (2 years) **Part Time** – 6 Semesters (3 years)	B E / B.Tech. in ECE / IT / EEE / CSE / ISE / TE / MCA / M.Sc. in Computer Science or Mathematics or Information Science or Information Technology with a minimum of 50% (45% in case of SC/ST) marks in aggregate of any recognized University / Institution or AMIE or any other qualification recognized as equivalent there to.
3	M Tech in Computer Aided Structural Engineering Construction Technology & Management Transportation Engineering and Management	4 Semesters (2 years)	BE/ B.Tech. in Civil Engineering with a minimum of 50% (45% in case of SC/ST) marks in aggregate of any recognized University / Institution or AMIE or any other qualification recognized as equivalent there to.
4	M Tech in Power Energy & Systems	4 Semesters (2 years)	BE/ B.Tech. in EE/ EEE/ ECE/ CSE/ MS / M.Sc. in Mathematics/Physics/Electronics / Information Technology or Information Science with a minimum of 50% (45% in case of SC/ST) marks in aggregate of any recognized University / Institution or AMIE or any other qualification recognized as equivalent there to.
5	M Tech in Digital Communication and Networking	4 Semesters (2 years)	B E / B.Tech. in ECE /TE / EEE / CSE / ISE / Instrumentation Technology / Medical Electronics/M Sc in Electronics with a minimum of 50% (45% in case of SC/ST) marks in aggregate of any recognized University/Institution or AMIE or any other qualification recognized as equivalent there to.
6	M Tech in VLSI and Embedded Systems	**Full Time** – 4 Semesters (2 years) **Part Time** – 6 Semesters (3 years)	B E / B.Tech. in ECE /TE / EEE / CSE / ISE / Instrumentation Technology / Medical Electronics/M Sc in Electronics with a minimum of 50% (45% in case of SC/ST) marks in aggregate of any recognized University/Institution or AMIE or any other qualification recognized as equivalent there to.
7	M Tech in Machine Design	4 Semesters (2 years)	BE / B.Tech. in Mechanical/Aeronautical / Automobile / Industrial Production Engineering with a minimum of 50% (45% in case of candidatebelonging to SC/ST category) marks in aggregate, of any recognized University / Institution or AMIE or any other qualification recognized as equivalent there to.

5.2 Provided further that the eligibility criteria are subject to revision by the Government Statutory Bodies, such as AICTE, UGC from time to time.

6. Courses of Study and Credits

6.1 Each course of study is assigned with certain credit value

6.2 Each semester is for a total duration of 20 weeks out of which 16 weeks dedicated for teaching and learning and the remaining 4 weeks for final examination, evaluation and announcement of results

6.3 The credit hours defined as below

In terms of credits, every one hour session of L amounts to 1 credit per Semester and a minimum of two hour session of T or P amounts to 1 credit per Semester or a three hour session of T / P amounts to 2 credits over a period of one Semester of 16 weeks for teaching-learning process.

1 credit = 13 credit hours spread over 16 weeks or spread over the semester

The total duration of a semester is 20 weeks inclusive of semester-end examination.

The following table describes credit pattern

Table-2: CreditPattern

Lectures(L)	Tutorials(T)	Practice (P)	Credits(L:T:P)	Total Credits	TotalContact Hours
4	2	0	4:1:0	5	6
3	2	0	3:1:0	4	5
3	0	2	3:0:1	4	5
2	2	2	2:1:1	4	6
0	0	6	0:0:3	3	6
4	0	0	4:0:0	4	4
2	0	0	2:0:0	2	2

a. The concerned BoS will choose the convenient Credit Pattern for every course based on size and nature of the course

7. Different C**ourses of Study**:

Different C**ourses of Study** are labeled as follows:

a. Core Course (CC)

b. Foundation Course (FC)
c. Hard Core Course (HC)
d. Soft Core Course (SC)
e. Open Elective Course (OE)
f. Minor Project
g. Major Project / Dissertation:

The credits for minor projects, major project/Dissertation will be decided by the respective Schools.

8. Credit and Credit Distributions:

8.1 A candidate has to earn 72 credits for successful completion of M Tech degree with a distribution of credits for different courses as prescribed by the University.

8.2 A candidate can enroll for a maximum of 24 credits per Semester. However s/he may not successfully earn a maximum of 24 credits per semester. This maximum of 24 credits does not include the credits of courses carried forward by a candidate.

8.3 **Only such full time candidates who register for a minimum prescribed number of credits in each semester from I semester to IV semester and complete successfully 72 credits in 4 successive semesters shall be considered for declaration of Ranks, Medals, Prizes and are eligible to apply for Student Fellowship, Scholarship, Free ships, and such other rewards / advantages which could be applicable for all full time students and for hostel facilities**.

9. Assessment and Evaluation

9.1 The assessment and evaluation process happens in a continuous mode. However, for reporting purpose, a Semester is divided into 3 components as IA1, IA2 and SEE. The performance of a candidate in a course will be assessed for a maximum of 100 marks as explained below.

(i) Component IA1:

The first Component (IA1), of assessment is for 25 marks. This will be based on test, assignment / seminar. During the first half of the semester (i.e. by 8th week), the first 50% of the syllabus (Unit 1&2) will be completed. This shall be consolidated during the first three days of 8th week of the semester. A review test based on IA1 will be conducted and completed in the beginning of the 9th week. In case of courses where test cannot be conducted, the form

of assessment will be decided by the concerned school and such formalities of assessment will be completed in the beginning of the 9th week. The academic sessions will continue for IA2 immediately after completion of process of IA1.

The finer split - up for the award of marks in IA1 is as follows:

Assignment & Seminars…….. 10 marks for the first 20% of the syllabus

Test (Mid-Term) ……..15 marks for the first 30% of the syllabus

Total …… ……..25 marks

(ii) Component IA2:

The second component (IA2), of assessment is for 25 marks. This will be based on test, assignment /seminar. The continuous assessment and scores of second half of the semester (9th to 16th week) will be consolidated during 16th week of the semester. During the second half of the semester the remaining units in the course will be completed. A review test based on IA2 will be conducted and completed during 16th week of the semester. In case of courses where test cannot be conducted, the form of assessment will be decided by the concerned school and such formalities of assessment will be completed during 16th week.

The 17th week will be for revision of syllabus and preparation for the semester – end examination.

The finer split - up for the award of marks in IA2 is as follows:

Assignment/Seminar……..10 marks for the second 20% of the syllabus

Review Test (Mid-Term) ……..15 marks for the second 30% of the syllabus

Total ……..25 marks

(iii) Component SEE:

The Semester End Examination of 3 hours duration for each course shall be conducted during the 18th & 19th week. **This forms the third / final component of assessment (SEE) and the maximum marks for the final component will be 50.**

9.2 The schedule of continuous assessment and examinations are summarized in the following Table below.

Component	Period	Syllabus	Weightage	Activity
IA1	1st Week to 8th Week	First 50% (two units)		Instructional process and Continuous Assessment
	Last 3 days of 8th Week		25%	Consolidation of IA1

IA2	9th week to 16th week	Second 50% (remaining two units)		Instructional process and Continuous Assessment
	Last 3 days of 16th week		25%	Consolidation of IA2
SEE	17th and 18th week			Revision and preparation for Semester end examination
	19th week to 20th week	Entire syllabus	50%	Conduct of semester end examination and Evaluation concurrently
	21st week			Notification of Final Grades
***Evaluation shall begin very first day after completion of the conduct of examination of the first course and both examination and evaluation shall continue concurrently. The examination results / final grades be announced latest by 21st week**				

Note: 1. Practical examination wherever applicable shall be conducted before conducting of IA2 examination. The calendar of practical examination shall be decided by the respective school.

2. Finally**, awarding the Grades** be announced latest by 5 days after completion of the examination.

9.3 The Assessment of MOOC and Online Courses shall be decided by the concerned School Board of Studies (BOS).

9.3.1 **For > 3 credit courses**

i	IA-I	25 marks
ii	IA-2	25 marks
iii	Semester end examination by the concern school board (demo, test, viva voice etc)	50 marks
	Total	**100 marks**

9.3.2 **For 1 & 2 credit courses**

i	IA-I	15 marks
ii	IA-2	15 marks
iii	Semester end examination by the concern school board (demo, test, viva voice etc)	20 marks
	Total	**50 marks**

9.3.3 The 50 marks meant for Internal Assessment (IA) of the performance in carrying out practical shall further be allocated as under:

i	Conduction of regular practical / experiments throughout the semester	20 marks
ii	Maintenance of lab records / Activities /Models / charts etc	10 marks
iii	Performance of mid-term test (to be conducted while conducting second test for theory courses); the performance assessments of the mid-term test includes performance in the conduction of experiment and write up about the experiment.	20 marks
	Total	**50 marks**

In case of an integrated course 20% marks be earmarked for laboratory work.

For example:

During IA1

Laboratory work …….. 10 marks

Test (Mid-Term) ……..15 marks for the first 50% of the theory syllabus

Total …… ……..25 marks

During IA2

Laboratory work …….. 10 marks

Test (Mid-Term) ……..15 marks for the second 50% of theory syllabus

Total …… ……..25 marks

SEE to be conducted for theory portions only and assessed for 50 marks

10. Setting Questions Papers and Evaluation of Answer Scripts:

10.1 There shall be three sets of questions papers set for each course. Two sets of question papers shall be set by the internal and one set by external examiner for a course. The Chairperson of the BoE shall get the question papers set by internal and external examiners.

10.2 The Board of Examiners shall scrutinize and approve the question papers and scheme of valuation.

10.3 There shall be double evaluation, viz, first valuation by the internal evaluator who has taught the course and second evaluation shall be an external examiner who is familiar with the course. The average marks of the two evaluations (internal examiner & external examiner) shall be the marks to be considered for declaration of results.

10.4 The examination for Practical work/ Field work/Project work will be conducted jointly by two examiners (internal and external). However, in case of non-availability of external examiner or vice versa, the Chairperson BoE at his discretion can invite internal / external examiners as the case may be, if required.

10.5 If a course is fully of (L=0):T: (P=0) type, then the examination for SEE Component will be as decided by the BoS concerned.

10.6 In case of a course with only practical component a practical examination will be conducted with two examiners and each candidate will be assessed on the basis of: a) Knowledge of relevant processes, b) Skills and operations involved, and c) Results / Products including calculation and reporting.

10.7 The duration for Semester-End practical examination shall be decided by the Controller of Examinations.

11. Evaluation of Minor Project / Major Project / Dissertation:

Right from the initial stage of defining the problem, the candidate has to submit the progress reports periodically and also present his/her progress in the form of seminars in addition to the regular discussion with the supervisor. At the end of the semester, the candidate has to submit final report of the project / dissertation, as the case may be, for final evaluation. The components of evaluation are as follows:

Component – I	(IA1)	Periodic Progress and Progress Reports (25%)
Component – II	(IA2)	Results of Work and Draft Report (25%)
Component– III	(SEE)	Final Evaluation and Viva-Voce (50%). Evaluation of the report is for 30% and the Viva-Voce examination is for 20%.

12. All assessments must be done by the respective Schools as per the guidelines issued by the Controller of Examinations. However, the responsibility of announcing final examination results and issuing official transcripts to the students lies with the office of the Controller of Examinations.

13. Requirements to Pass a Course

13.1 A candidate's performance from all 3 components will be in terms of scores, and the sum of all three scores will be for a maximum of 100 marks (25 + 25 + 50). A candidate who secures a minimum of 40% in the SEE and an overall 40% (IA1+IA2+SEE) in a course is said to be successful.

13.2 **The Grade and the Grade Point:** The Grade and the Grade Point earned by the candidate in the subject will be as given below:

Marks, P	Grade, G	Grade Point (GP=V x G)	Letter Grade
90-100	10	v*10	O
80-89	9	v*9	A+
70-79	8	v*8	A
60-69	7	v*7	B+
55-59	6	v*6	B
50-54	5.5	v*5.5	C+
40-49	5	v*5	C
0-39	0	v*0	F
ABSENT			AB

O - Outstanding; A+-Excellent; A-Very Good; B+-Good; B-Above Average; C+-Average; C-Satisfactory; F – Unsatisfactory.

Here, P is the percentage of marks (P=[(IA1+IA2)+SEE] secured by a candidate in a course which is **rounded to nearest integer**. v is the credit value of course. G is the grade and GP is the grade point.

a. Computation of SGPA and CGPA

The Following procedure to compute the Semester Grade Point Average (SGPA)

The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e

SGPA (Si) = ∑(Ci x Gi) / ∑Ci

Where Ci is the number of credits of the ith course and Gi is the grade point scored by the student in the ith course.

b. Illustration for Computation of SGPA and CGPA

Illustration No. 1

Course	Credit	Grade letter	Grade Point	Credit Point (Credit x Grade)
Course 1	**3**	**A**	**9**	**3X9=27**
Course 2	**3**	**B**	**8**	**3X8=24**
Course 3	**3**	**C**	**7**	**3X7=21**

Course 4	**3**	**O**	**10**	**3X10=30**
Course 5	**3**	**D**	**6**	**3X6=18**
Course 6	**3**	**O**	**10**	**3X10=30**
Course 7	**2**	**A**	**9**	**2X 9 = 18**
Course 8	**2**	**B**	**8**	**2X 8 = 16**
	22			**184**

Thus, **SGPA = 184 ÷ 22 = 8.36**

c. Cumulative Grade Point Average (CGPA):

Overall Cumulative Grade Point Average (CGPA) of a candidate after successful completion of the required number of credits (72) for two year post graduate degree in a specialization is calculated taking into account all the courses undergone by a student over all the semesters of a program, i. e **CGPA = ∑(Ci x Si) / ∑Ci**

Where Si is the SGPA of the ith semester and Ci is the total number of credits in that semester.

The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

Illustration:

CGPA after Final Semester

Semester (ith)	**No. of Credits (Ci)**	**SGPA (Si)**	**Credits x SGPA (Ci X Si)**
1	22	8.36	22 x 8.36 = 183.92
2	22	8.54	22 x 8.54 =187.88
3	16	9.35	16x9.35=149.6
4	12	9.50	12x9.50=114
Cumulative	**72**		635.4

$$CGPA = \frac{22\ X8.36 + 22\ X\ 8.54 + 16X9.35 + 12X9.5}{72} = 8.33$$

13.3 **Conversion of Grades Into Percentage:**

Conversion formula for the conversion of CGPA into Percentage is:

Percentage of marks scored = CGPA Earned x 10

Illustration: CGPA Earned 8.83 x 10=88.30

14. Classification of Results

The final grade point (FGP) to be awarded to the student is based on CGPA secured by the candidate and is given as follows:

CGPA	Grade (Numerical Index)	Letter Grade	Performance	FGP
	G			Qualitative Index
9 >= CGPA 10	10	O	Outstanding	Distinction
8 >= CGPA < 9	9	A+	Excellent	
7 >= CGPA < 8	8	A	Very Good	First Class
6 >= CGPA < 7	7	B+	Good	
5.5> = CGPA < 6	6	B	Above average	Second Class
> 5 CGPA < 5.5	5.5	C+	Average	
> 4 CGPA <5	5	C	Satisfactory	Pass
< 4 CGPA	0	F	Unsatisfactory	Unsuccessful

Overall percentage=10*CGPA

a. **Provisional Grade Card:** The tentative / provisional Grade Card will be issued by the Controller of Examinations at the end of every Semester indicating the courses completed successfully. The provisional grade card provides **Semester Grade Point Average** (SGPA).This statement will not contain the list of DROPPED courses.

b. **Final Grade Card:** Upon successful completion of the Post Graduate Degree a Final Grade card consisting of grades of all courses successfully completed by the Candidate will be issued by the COE.

15. Attendance Requirement:

15.1 All students must attend every lecture, tutorial and practical classes.

15.2 In case a student is on approved leave of absence (e g:- representing the University in sports, games or athletics, placement activities, NCC, NSS activities and such others) and / or anyother such contingencies like medical emergencies, the attendance requirement shall be minimum of 75% of the classes taught.

15.3 Any student with less than 75% of attendance in aggregate of all the courses including practical courses / field visits etc., during a semester shall not be permitted to appear to the end semester examination and such student shall seek re-admission

16. Re-Registration and Re-Admission:

16.1 In case a candidate's class attendance in aggregate of all courses in a semester is less than 75% or as stipulated by the University, such a candidate is considered as dropped the semester and is not allowed to appear for semester end examination and he / she shall have to seek re-admission to that semester during subsequent semester / year within a stipulated period.

16.2 In such case where in a candidate drops all the courses in a semester due to personal reasons, it is considered that the candidate has dropped the semester and he / she shall seek re-admission to such dropped semester.

17. Absence during Internal Test:

In case a student has been absent from an internal tests due to the illness or other contingencies he / she may give a request along with necessary supporting documents and certification from the concerned class teacher / authorized personnel to the concerned Director of the School, for conducting a separate internal test. The Director of the School may consider such request depending on the merit of the case and after consultation with course instructor and class teacher, and arrange to conduct a special internal test for such candidate(s) well in advance before the Semester End Examination of that respective semester. Under no circumstances internal tests shall be held / assignments are accepted after Semester End Examination.

18. Eligibility to Appear for Semester End Examination (SEE)

18.1 Only those students who fulfill 75% attendance requirement and who secure minimum 30% marks in IA1 and IA2 together in a course are eligible to appear for SEE examination in that course.

18.2 Those students who have 75% of attendance but have secured less than 30% marks in IA1 and IA2 together in a course are not eligible to appear for SEE examination in that course. They are treated as dropped the course and they will have to repeat that course whenever it is offered.

18.3 In case a candidate secures more than 30% in IA1 and IA2 together but less than 40% in aggregate of IA1, IA2 and SEE in a course is considered as unsuccessful and such a candidate may either opt to DROP that course or appear for SEE examination during the subsequent semesters / years within the stipulated period.

18.4 In such a case wherein he / she opts to appear for just SEE examination, then the marks secured in IA1 and IA2 shall get continued. Repeat SEE examination will be conducted in respective semesters.

19. Provision for Supplementary Examination

In case a candidate fails to secure a minimum of 40% (20 marks) in Semester End Examination (SEE) and a minimum of 40% marks overall (IA and SEE together), such candidate shall seek supplementary examination of only such course(s) wherein his / her performance is declared unsuccessful. The supplementary examinations are conducted after the announcement of even semester examination results. The candidate who is unsuccessful in a given course(s) shall appear for supplementary examination of odd and even semester course(s) to seek for improvement of the performance.

20. Provision to Carry Forward the Failed Subjects / Courses:

A candidate who secures a minimum of 40% in the SEE and an overall 40% (IA1+IA2+SEE) in a course is said to be successful otherwise considered that the candidate has failed the course. A candidate is required to successfully complete all the courses before submission of major project report or dissertation report.

(It means that the candidate has no restrictions on the number of courses that can be carried forward)

21. Provision for Appeal

If a candidate is not satisfied with the evaluation of Internal Assessment components (Internal Tests and Assignments), he/she can approach the Grievance Cell with the written submission together with all facts, the assignments, and test papers, which were evaluated. He/she can do so before the commencement of respective semester-end examination. The Grievance Cell is empowered to revise the marks if the case is genuine and is also empowered to levy penalty as prescribed by the University on the candidate if his/her submission is found to be baseless and unduly motivated. This Cell may recommend for taking disciplinary/corrective action on an evaluator if he/she is found guilty. The decision taken by the Grievance committee is final.

22. Grievance Committee:

In case of students having any grievances regarding the conduct of examination, evaluation and announcement of results, such students can approach Grievance Committee for redressal

of grievances. Grievance committees will be formed by CoE in consultation with VC

For every program there will be one grievance committee. The composition of the grievance committee is as follows:-

- The Controller of Examinations - Ex-officio Chairman / Convener
- One Senior Faculty Member (other than those concerned with the evaluation of the course concerned) drawn from the school / department/discipline and/or from the sister schools / departments/sister disciplines – Member.

- One Senior Faculty Members / Subject Experts drawn from outside the University school / department – Member.

23. With regard to any specific case of ambiguity and unsolved problem, the decision of the Vice-Chancellor shall be final.

REVA UNIVERSITY
Bengaluru, India

School Of Electronics and Communication Engineering

Scheme Of Instructions

I Semester								
Sl. No.	**Course Code**	**Title of the Course**	**HC/FC/SC /OE**	**Credit Pattern**				**Contact Hours/Week**
				L	**T**	**P**	**Total**	
1	M20AS0101	Advanced Mathematics	HC	3	0	0	3	3
2	M20TL0103	CMOS VLSI Design	HC	3	0	1	4	5
3	M20TL0102	Advanced Embedded System Design	HC	3	0	1	4	5
4	M20TL0101	Advanced Digital System Design using Verilog	HC	2	0	1	3	4
5	M20TL0104	Communication Busses and Interfaces	HC	3	0	0	3	3
6	M20TL0105	Internet of Things- Practical Approach using NXP Rapid IoT Kit	HC	3	0	0	3	3
						Total Credits	**20**	**23**
SECOND SEMESTER								
1	M20TL0201	Design of Analog CMOS Integrated Circuits	HC	3	0	1	4	5
2	M20TL0202	Real Time Operating Systems	HC	3	0	1	4	5
3	M20TLS0211	VLSI Testing	SC1	3	0	0	3	3
	M20TLS0212	Semiconductor Device Modeling & Technology		3	0	0		
	M20TLS0213	IC Fabrication		3	0	0		
	M20TLS0214	ASIC Design		3	0	0		
	M20TLS0215	Static Timing Analysis		3	0	0		
4	M20TLS0221	Unix/Linux Shell Scripting and Python Basics	SC2	3	0	0	3	3
	M20TLS0222	SOC Design		3	0	0		
	M20TLS0223	Embedded Systems For Automotive Applications		3	0	0		
	M20TLS0224	Advanced Computer Architecture		3	0	0		

	M20TLS0225	Designing With Power Devices		3	0	0		
5	M20TLS0231	Nanoelectronics	SC3	3	0	0	3	3
	M20TLS0232	VLSI for Signal Processing		3	0	0		
	M20TLS0233	Low Power VLSI Design		3	0	0		
	M20TLS0234	MEMS		3	0	0		
	M20TLS0235	High Speed VLSI Design		3	0	0		
6	M20TLS0241	ASIC Design and Verification using SystemVerilog	SC4	3	0	0	3	3
	M20TLS0242	Embedded Applications In Power Conversion		3	0	0		
	M20TLS0243	Product Design & Quality Management		3	0	0		
	M20TLS0244	Embedded Systems In Smart Grid		3	0	0		
	M20TLS0245	Embedded Linux System Design And Development		3	0	0		
						Total	**20**	**22**

Sl. No.	**Course Code**	**Title of the Course**	**Course Type**	**Credit Pattern**				**Contact Hours/Week**
				L	**T**	**P**	**Total**	
		THIRD SEMESTER						
1	M20TLS0311	Blended learning: Electronic Packaging	SC5	3	0	0	3	3
	M20TLS0312	Blended learning: Algorithms For VLSI		3	0	0		
	M20TLS0313	Blended learning: Synthesis and optimization of Digital Circuits		3	0	0		
	M20TLS0314	Blended learning: CMOS RF Circuit Design		3	0	0		
	M20TLS0315	Advances in VLSI Design		3	0	0		
2	M20TLO0301	Suitable online course	OE	3	0	0	3	3
3	M20TL0101	Project Phase-1	HC	0	0	4	4	8
4	M20TL0102	Internship	-	0	0	6	6	12
						Total	**16**	**26**
		FOURTH SEMESTER						
1	M20TL0401	Project Phase II Dissertation&Masters Thesis	HC**	0	0	16	16	32

Total	**16**	**32**
Total Credits for four Semesters	**72**	

Note: HC = Hard Core: SC= Soft Core
*For all the courses which are not supported by lab component students have to build mini project and it has to be evaluated.
**Mandatory to publish the outcome of project work into research article in reputed journals as specified by the project guide.

Detailed Syllabus

Semester – I

<table>
<tr><td colspan="2">Course Title</td><td colspan="4">Advanced Mathematics</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td colspan="2">Course Code</td><td>M20AS0101</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">I Semester</td></tr>
<tr><td rowspan="5">Advanced Mathematics</td><td>TLP</td><td>Credits</td><td colspan="2">Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td colspan="2">3</td><td>3</td></tr>
<tr><td>Practice</td><td>0</td><td colspan="2">0</td><td>0</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td colspan="2">-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td colspan="2">3</td><td>3</td><td>39</td><td>0</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

There are three parts in this course: first is the advanced matrix theory which comprises of QR-decomposition and singular value decomposition, second part consists of Calculus of variation i.e., applications of Euler's equations, Laplace and Fourier transformations and the last section is optimization of linear and non linear programming problems. Basically QR-decomposition or QR-factorization is a linear algebra operation that factors a matrix into an orthogonal component, which is a basis for the row space of the matrix, and a triangular component. In adaptive signal processing, the QR is often used in conjunction with a triangular solver. The singular value decomposition is a method of decomposing a matrix into three other matrices as given below:$A = USV^T$ where A is a $m \times n$utility matrix, U is a $m \times r$orthogonal left singular matrix, which represents the relationship between users and latent factors, S is a $r \times r$diagonal matrix, which describes the strength of each latent factor and V is a $r \times n$diagonal right singular matrix, which indicates the similarity between items and latent factors. Mathematical applications of the SVD include computing the pseudoinverse, matrix approximation, and determining the rank, range, and null space of a matrix. The SVD is also extremely useful in all areas of science, engineering, and statistics, such as signal processing, least squares fitting of data, and process control.

Differential equations can be obtained by Laplace transformation, which converts differential equation into an algebraic equation with incorporation of the boundary conditions from the beginning. Also non-periodic function can be represented as an integral over a continuous range of frequencies. The concept of Laplace Transformation and Fourier Transformation play a vital role in diverse areas of science and technology such as electric analysis, communication engineering, control engineering, linear system, analysis, statistics, optics, quantum physics, solution of partial differential operation, etc. In solving problems relating to these fields, one usually encounters problems on time invariants, differential equations, time and frequency domains for non-periodic wave forms.

Third section consist of optimization technique which consists of linear and non-linear programming problem: As energy and equipment costs increase, efficient energy systems become more important in the overall economics of process plants.A linear and non-linear programming method is used to minimize the total costs for energy used net costs in steam-condensing systems.

COURSE OBJECTIVES:

The objectives of this course are:

1. Make the students to understand advanced matrix theory which are applicable to signal processing, statistics, least squares fitting of data and process control.
2. Make the students to understand the numerical, analytical and logical problem solving using Euler's equations.
3. To make understand the concept and applications of Laplace and Fourier transforms, solving elliptic equation using transform methods.
4. Study the concepts of linear and nonlinear programming and its applications.

COURSE OUTCOMES(COs)
On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Identify and describe different techniques in solving Engineering problems using Matrix method.	1,2,3	1,3
CO2	Describe the Euler equation of first and higher order degree.	1,2,3	1,3
CO3	Apply Laplace transform and Fourier transform to one dimensional wave and two dimension heat and wave equations. . .	1,2,3	1,3
CO4	Applications of Simplex method, dual simplex, Two Phase and Big M techniques for LPP and solving non linear programming problem using Kuhn- Tucker and Lagrange's multiplier method.	1,2,3	1,3
CO5	Solving the real time examples using transform method	1,2,3	1,3
CO6	Describe the linear and non linear systems with an examples	1,2,3	1,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓	✓	✓		
CO2	✓	✓	✓			
CO3	✓	✓	✓			
CO4	✓	✓	✓	✓		
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	3									1		2
CO2	3	3	2									2		1
CO3	1	3	2									2		1
CO4	2	3	1									2		1

CO5														
CO6														

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT – 1 **Matrix Theory:** QR-Decomposition, Eigen values using shifted QR algorithm, Singular Value Decomposition (SVD), Pseudo inverse, Least square approximations.
UNIT – 2 **Calculus of Variations**: Concept of Functional, Euler's equation, functional dependent on first and higher order derivatives. – Functional on several dependent variables – Isoperimetric problems, Variation problems with moving boundaries.
UNIT – 3 **Transform Methods and Elliptic Equation:** Laplace transform methods for one dimensional wave equation, Displacements in a string, Longitudinal vibration of an elastic bar, Fourier Transform methods for one dimensional heat conduction problems in infinite and semi-infinite rod. Laplace equation, Properties of harmonic functions, Fourier transforms methods for Laplace equations. Solution for Poisson equation by Fourier transforms method.
UNIT – 4 **Linear and Non Linear Programming:** Simplex Algorithm, Two Phase and Big-M techniques, Duality theory- Dual Simplex method. Non Linear Programming Constrained external problems, Lagrange's multiplier method, Kuhn- Tucker conditions and solutions. Recent trends in the related areas from journals, Conference proceedings Book chapters.

References:

1. Richard Bronson, "**Schaum's Outlines of Theory and Problems of Matrix Operations**", McGraw-Hill, 1988.
2. Venkataraman M. K., "**Higher Engineering Mathematics**", National Publications Co., 1992.

3. Elsgolts, L., "**Differential Equations and Calculus of Variations**", Mir, 1977.
4. Sneddon, I.N., "**Elements of Partial Differential Equations**", Dover Publications, 2006.
5. Sankara Rao, K., "**Introduction to Partial Differential Equations**", Prentice – Hall of India,1995.
6. Taha H A, "**Operations Research - An Introduction**", McMilan Publishing co, 1982.

<table>
<tr><td colspan="2">Course Title</td><td colspan="4">CMOS VLSI DESIGN</td><td colspan="2">Course Type</td><td colspan="2">Integrated</td></tr>
<tr><td colspan="2">Course Code</td><td>M20TL0103</td><td>Credits</td><td colspan="2">4</td><td colspan="2">Class</td><td colspan="2">I Semester</td></tr>
<tr><td rowspan="5">CMOS VLSI DESIGN</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>1</td><td>2</td><td>2</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>4</td><td>5</td><td>5</td><td>39</td><td>26</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

The course starts with basic device understanding and then deals with complex digital circuits, good scalability keeping in mind the current trend in technology. Also Implementation strategies, architecture of memory arrays.

COURSE OBJECTIVES:
The objectives of this course are:

1. Understand an overview of working principle of MOS transistor and MOS inverters.
2. Know the concepts of power estimation and delay calculations in CMOS circuits.
3. Learn the different types of memory circuits and their design.
4. Study chip input output devices.

COURSE OUTCOMES(COs)
On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Demonstrate the fundamentals of IC technology components, scaling trends, and limitations.	1,2,3,4,5,6,9, 10	1,2,3

CO2	Analyze the switching characteristics of MOS inverter.	1,2,4,5,6,9,10	1,2,3
CO3	Understand the semiconductor memory operation and explore the power optimization	1,2,4,5,6,9,10	1,2,3
CO4	Understand chip input-output devices and modules.	1,2,3,4,9,10	1,2,3
CO5	Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	1,2,3,4,9,10	1,2,3
CO6	Use Bipolar and Bi-CMOS circuits in very high speed design.	1,2,3,4,9,10	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1		✓				
CO2				✓		
CO3				✓		
CO4				✓		
CO5		✓				
CO6		✓				

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	1			3	3		1	3	2
CO2	2	3		1	1	1			3	3		1	3	2
CO3	3	3		2	1	2			3	3		2	3	2
CO4	3	3		3					3	3		3	3	2
CO5	1	3		2					1	1		3	3	2
CO6	2	3		1					1	1		3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents

UNIT – 1

MOS Transistor, MOS Inverters:The Metal Oxide Semiconductor (MOS) Structure, the MOS System under External Bia Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, and MOSFET Scaling and Small-Geometr Effects.
Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with type MOSFET Load, CMOS Inverter.

UNIT - 2

MOS Inverters (continued):Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation o Delay Times, and Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, an Switching Power Dissipation of CMOS Inverters.

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

UNIT - 3

Semiconductor Memories :Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). Low-Power CMOS Logic Circuit Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization o Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits.

BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJT Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

UNIT - 4

Chip Input and Output (I/O) Circuits:Introduction, ESD Protection, Input Circuits, Output Circuits and L (di/dt) Noise, On-Chi Clock Generation and Distribution, Latch-Up and Its Prevention.

Design for Manufacturability : Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments an Performance Modeling, Parametric Yield Estimation, Parametric Yield Maximization, Worst-Case Analysis, Performanc Variability Minimization.

PRACTICE SESSION:

Sl. No.	**Name of the Practice Session**	**Tools and Techniques**	**Expected Skill /Ability**
1	NMOS input, output characteristics with parametric sweep 1. Input and output characteristics 2. Varying Lamda, Id Vs Vds 3. Varying the aspect ratio	Cadence Virtuoso tool	Design schematic and perform analysis while working in a team.

2	Study of MOS inverter with resistive load 1. Inverter DC characteristics 2.Variying the resistive load and aspect ratio	Cadence Virtuoso tool	Design schematic and perform analysis while working in a team.
3	Study of CMOS Inverter 1. Transient response. 2. DC response 3. parametric analysis	Cadence Virtuoso tool	Design schematic and perform analysis while working in a team.
4.	Study of Inverter with depletion load NMOS 1. DC characteristics 2. Transient response 3. Transient response with varying the width and length of the driver	Cadence Virtuoso tool	Design schematic and perform analysis while working in a team.
5.	Study of CMOS gates 1. NAND/ AND Gate 2. NOR/ OR Gate 3. XOR/ XNOR gate	Cadence Virtuoso tool	Design schematic and perform analysis while working in a team.

TEXT BOOKS:

1. 1. Sung Mo KangandYosufLeblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition, 2003.
2. 2. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

JOURNALS/MAGAZINES/ ADDITIONAL SOURCES:

1. https://ieeexplore.ieee.org/abstract/document/536820
2. https://www.degruyter.com/document/doi/10.1515/ntrev-2017-0155/html
3. https://www.sciencedirect.com/topics/engineering/metal-oxide-semiconductor-field-effect-transistor
4. https://www.sciencedirect.com/science/article/abs/pii/0308595376900027
5. https://www.sciencedirect.com/topics/computer-science/bipolar-junction-transistor
6. http://web.engr.uky.edu/~elias/lectures/In_15.pdf
7. https://www.sciencedirect.com/science/article/abs/pii/S0026269283800068

SWAYAM/NPTEL/MOOCs:

1. https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ee25/
2. https://nptel.ac.in/courses/108/107/108107129/
3. https://nptel.ac.in/courses/108/107/108107142/
4. https://nptel.ac.in/content/storage2/courses/117101058/downloads/Lec-33.pdf

Course Title	Advanced Embedded Systems Design				Course Type		Integrated	
Course Code	M20TL0102	Credits	4		Class		I Semester	
Advanced Embedded Systems Design	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	1	2	2				
	-	-	-	-	Theory	Practical	IA	SEE
	Total	**4**	**5**	**5**	**39**	**26**	**50 %**	**50 %**

COURSE OVERVIEW:

An Advanced course in Embedded System design utilizing ARM (Advanced RISC Machine) cortex processor is a reduced instruction set computing architecture for computer processors, configured for various environments. This Course will discuss the basic concepts of embedded system design, with particular emphasis on system design using ARM microcontrollers. Keeping in view of the recent developments, this course will be based on state-of-the-art microcontroller boards and programming environments.

This course is tailored and designed to deliver sound theoretical and practical skills in the field of ARM based embedded systems. This course will help in gaining knowledge in understanding the architecture of ARM to establish as a leader in the industry.

COURSE OBJECTIVES:

The objectives of this course are:

1. To understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Describe the hardware software co-design and firmware design approaches
3. To illustrate the architectural features and instruction set of ARM Cortex-M3 Processors
4. To program ARM cortex M3 using various assembly instructions and C language.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	1,2,3,4,5,6,9, 10,11	1,2,3
CO2	To identify different functional blocks in an ARM Microcontroller and their Applications.	1,2,3,4,9,10	1,2,3
CO3	Program ARM Cortex-M3 MCUs by identifying the software development tools.	1,2,3,4,5,9,1 0,11	1,2,3
CO4	Select a proper Microcontroller for a particular application.	1,2,3,4,6, 9,10,11	1,2,3
CO5	Acquire the knowledge of the architectural features of ARM CORTEX M3, 32-bit microcontroller including memory map, interrupts and exceptions.	1,2,3,4,5,9,1 0,11	1,2,3
CO6	Apply the knowledge gained for Programming ARM CORTEX M3 for differen applications	1,2,3,4,5,10, 11	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1			✓			
CO2					✓	
CO3				✓		
CO4			✓			
CO5				✓		
CO6						✓

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	2	2	2			2	2	1	2	3	2
CO2	2	1	2	3					3	3		2	3	2
CO3	3	2	1	2	2				3	3	2	2	3	2
CO4	1	3	3	1		3			2	1	3	2	3	2
CO5	3	2	1	2	2				2	3	2	2	3	2
CO6	3	2	1	2	2				2	3	2	2	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents

UNIT - 1

Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.

UNIT - 2

Embedded System Concepts and Introduction to ARM: Hardware Software Co-Design, embedded firmware design approaches computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware Components in embedded system development environment (IDE), Development and debugging Tools**.**

ARM Architecture

Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.

UNIT - 3

Introduction to Cortex-M3 Processor :Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register,Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector
Tables, Stack Memory Operations, Reset Sequence.
Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions.

UNIT - 4

Cortex-M3Programming: Cortex-M3 Implementation Overview: Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus. Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface. Systick Timer,

Interrupt Behaviour: Exceptions, Nested Vector interrupt controller design, Exceptions exit, tail chaining interrupt, late arrivals an interrupt latency Cortex-M3 Programming using assembly and C language, CMSIS

PRACTICE SESSION:

Sl. No.	Name of the Practice Session	Tools and Techniques	Expected Skill /Ability
1	Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM =10+9+8+.....+1	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
2	Write an Assembly language program to store data in RAM	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
3	Write a C program to output the “Hello World” message using UART	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
4	Write a C program to operate a buzzer using Cortex M3	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
5	Write a C program to control stepper motor using Cortex M3.	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
6	Interface an External Push Button Switch, LED with MCU target board,andWrite aC Program to Configure and Control the ON-OFF operation of the LED using the switch. (Configure Switches an External interrupt source)	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
7	Interface a4x4 Matrix Keypad, LED’s Array with MCU target board, and Write a C program to display the binary equivalent pattern of the numeric key pressed on the LEDsarray.	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	ARM Cortex Programming using ALP and C Programming
8	Interface a 16x2 LCD for its 4 bit mode operation, with MCU target board and Write a C Program to display a message on both the lines ofthe LCD.	ARM Cortex M3/M4Evaluation Board, KeiluVision 4	Design and circuit debugging. Working in a team
9	Write a C Program to Configure the on-chip UART functional block of the MCU target board to output a message on serial terminal of	ARM Cortex M3/M4 Evaluation Board,	Design and circuit debugging.

	a host machine via its serial/ COM port.	KeiluVision 4	Working in a team
10	Verification of basic logic gates using discrete components	ARM Cortex M3/M4 Evaluation Board, KeiluVision 4	Design and circuit debugging. Working in a team

TEXT BOOKS:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd edn, Newnes, (Elsevier), 2010.

REFERENCE BOOK:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.
2. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England;Morgan Kaufmann Publishers
3. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide -Designing and Optimizing System Software", 2006, Elsevier.
4. Raghunandan G H "Microcontroller (ARM) and Embedded Systems", 1st edition 2020, ISBN: 9789353504106, Cengage Publications

JOURNALS/MAGAZINES/ ADDITIONAL SOURCES:

1. https://www.arm.com/resources/education/online-courses
2. https://class.ece.uw.edu/474/peckol/doc/StellarisDocumentation/IntroToCortex-M3.pdf
3. https://www.nielit.gov.in/aurangabad/content/certificate-course-embedded-system-design-using-arm-cortex-microcontroller-0
4. http://courseware.cutm.ac.in/courses/2285/

SWAYAM/NPTEL/MOOCs:

1. https://nptel.ac.in/courses/106/105/106105193/
2. https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-cs15/
3. https://www.udemy.com/course/embedded-system-programming-on-arm-cortex-m3m4/

<table>
<tr><td colspan="2">Course Title</td><td colspan="4">Advanced Digital System Design using Verilog</td><td colspan="2">Course Type</td><td colspan="2">Integrated</td></tr>
<tr><td colspan="2">Course Code</td><td>M20TL0101</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">I Semester</td></tr>
<tr><td rowspan="5">Advanced Digital System Design using Verilog</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>2</td><td>2</td><td>2</td></tr>
<tr><td>Practice</td><td>1</td><td>2</td><td>2</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>4</td><td>4</td><td>26</td><td>26</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

This course covers the systematic design of advanced digital systems using field-programmable gate arrays (FPGAs). Topics covered will focus on the design of digital systems using combinational, sequential, and UDP's. Techniques for logic design, including asynchronous logic, physical world interfaces to digital systems, and system

performance analysis methods will be studied. Advanced methods of logic minimization and state-machine design are discussed.

COURSE OBJECTIVES:

The objectives of this course are:

1. Understand the concepts of Verilog Language. Also, design the digital systems as an activity in a larger systems design context.
2. Analyze the HDL language feature to realize the complex digital systems.
3. Study the design and operation of Sequential circuits, semiconductor memories frequently used in digital system.
4. Provide an Understanding to concepts FSM basics.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Design & Construct the combinational circuits using discrete gates and programmable logic devices.	1,2,3,4,5, 9,11	1,2,3
CO2	Describe Verilog hardware description languages (HDL) using Functions tasks and User-Defined Primitives	1,2,3,4,5,9,10	1,2,3
CO3	Construct the UDP for combinational and sequential circuits	1,2,3,4,5, 9,10	1,2,3
CO4	Understand and analyze the programming of sequential circuits using Verilog HDL.	11,2,3,4,5, 9,10	1,2,3
CO5	Explore the different types of FSM techniques.	1,2,3,4,5, 9,10	1,2,3
Co5	Explore the PLA and PLD in VLSI technology	1,2,3,4, 9,10	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓	✓			
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓		
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓	✓	✓	
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	3	2	1	2		3	2		1	2	1

CO2	3	3	3	1	2	3		3	3			3	2	1
CO3	3	3	2	3	3		1	2	3	3		3	3	2
CO4	3	3	2	3	3		1	2	3	3		3	3	1
CO5	3	3	2	3	3				1	1		3	3	1
CO6	3	3	2	3					1	1		3	3	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1 **Introduction to Digital System and Methodology** Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Design Methodology. Gate-level combinational circuit:Introduction, General description, Basic lexical elements and data types, Data types, Program skeleton, Structural description, Test bench. Overview of FPGA and EDA software:Introduction, Architecture of FPGA, Development flow, HDL for combinational Circuits, Design of Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter.
UNIT - 2 **Functions tasks and User defined Primitives:** Introduction, functions, tradeoff between hardware and speed, scope of functions, recursive functions, tasks, task definition, task enabling, user defined primitives, combinational UDPs, More general combinational UDPs, Instantiation of UDP, Combinational UDP and Function, Sequential UDPs, UDP instantiation with delays, vector type instantiation of UDP
UNIT - 3 **Sequential Basics**Storage Elements, Flip-flops and Registers, Shift Registers, Latches, Sequential Data paths and Control, Finite-State Machines, Clocked Synchronous Timing Methodology, Asynchronous Inputs, Verification of Sequential Circuits, Asynchronous Timing Methodologies,
UNIT - 3 Memories: General Concepts Memory Types, Asynchronous Static RAM Synchronous Static RAM, Multiport Memories, Dynamic RAM, Read - Only Memories.
UNIT - 4 **Queues, PLAS, Compiler directives and FSMS:** File based tasks and functions, compiler directives, time related tasks, queues, PLDs, programming PLD in Verilog, Design of finite state machine- Moore machine, Melay machine.

PRACTICE SESSION:

Sl. No.	**Name of the Practice Session**	**Tools and Techniques**	**Expected Skill /Ability**
1	**Write Verilog code for the design of 8-bit** i. Carry Ripple Adder ii. Carry Look Ahead adder iii. Carry Skip Adder	Xilinx IDE, FPGA board	Design and circuit debugging. Working in a team

2	**Write Verilog Code for 8-bit** i. Array Multiplication (Signed and Unsigned) ii. Booth Multiplication (Radix-4)	Xilinx IDE, FPGA board	Design and circuit debugging. Working in a team
3	**Write Verilog code for 4/8-bit** i. Magnitude Comparator ii. LFSR iii. Parity Generator iv. Universal Shift Register	Xilinx IDE, FPGA board	Design and circuit debugging. Working in a team
4	Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with and without overlap) any sequence can be specified.	Xilinx IDE, FPGA board	Design and circuit debugging. Working in a team
5	**Static Timing Analysis:** Synthesize the following listed digital systems and perform the timing analysis for 25MHz. Use the appropriate EDA tool- Xilinx a. 16 bit synchronous/Asynchronous counter b. 4:16 Decoder c. 32 bit carry ripple adder d. 32 Multiplier	Xilinx IDE, FPGA board	Design and circuit debugging. Working in a team

Text Books:

1. T.R. Padmanabhan, B. Bala Tripura Sundari , Design through Verilog HDL", Wiley Publication.
2. Pong P Chu, "FPGA Prototyping by Verilog Examples", Wiley, 2006.

Reference Books:

1. Frank Vahid, "Digital Design", Wiley, 2006.

<table>
<tr><td>Course Title</td><td colspan="3">Communication Busses and Interfaces</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td>Course Code</td><td>M20TL0104</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">I Semester</td></tr>
<tr><td rowspan="6">Communication Busses and Interfaces</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

Working with microcontrollers or any other electronic equipment involves working with interfaces, the electronic circuits that connect one device to another for communications. If you are designing electronic equipment, you have probably already worked with one or more interfaces. The most common wired interfaces, for example, are USB and HDMI in consumer equipment and RS-232/RS-485 in industrial equipment. However, there are dozens of others, some of which may not be familiar. Over the years, many new serial interfaces have been developed for specific purposes. This book attempts to catalog all of the more common well-known interfaces, both wired and wireless. This compendium of interfaces will serve as a guide for selecting, comparing, and using serial interfaces.

COURSE OBJECTIVES:

The objectives of this course are:

1. Discuss the possible option for designing the systems using IC's various communication busses.
2. Explain the architecture and protocols of the communication buses.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Decide the best possible option for designing the systems using IC's various communication busses.	1,2,3,4,5,6,7,8	1,2,3
CO2	Compare the various architecture and protocols of the communication buses.	1,2,3,4,5,6,7,8,9	2,3
CO3	Summarize and categorize the various communication bus protocols.	1,2,6,9	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓				
CO3	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	1	1	1				1	3	2
CO2	3	3	3	1	1	1	2	2	2				3	2
CO3	3	3				2			1			2	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents

UNIT - 1
Low-Speed Interfaces1-Wire, C-Bus, Controller Area Network (CAN), Inter-Integrated Circuit (I2C) Bus, Inter-IC Sound (I2S) Bus, RS-232, RS-485.
UNIT - 2
Medium-Speed Interfaces Ethernet, Joint Test Action Group (JTAG), Serial Peripheral Interface (SPI), Universal Serial Bus (USB)
UNIT - 3
High-Speed Interfaces DisplayPort (DP), Gigabit Ethernet (GE), Fibre Channel (FC), High-Definition Multimedia Interface (HDMI), PCI Express (PCIe), Serial Advanced Technology Attachment (SATA)
UNIT - 4
Broadband Interfaces and Wireless Interfaces Broadband Interface Concepts, Digital Subscriber Line (DSL), Bluetooth (BT), Near Fiel Communications (NFC), Wi-Fi, ZigBee

TEXT BOOKS:

1. Louis E. Frenzel Jr, "Handbook of SERIAL COMMUNICATIONS INTERFACES", 1ST Edition, Elsevier, 2015.
2. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports forEmbedded Systems", 2nd Edition, Lakeview Research, 2007.
3. Jan Axelson, "USB Complete", 5th Edition, Penram Publications, 2007.
4. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press, 2012.
5. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", 2nd Edition, Copperhill Media Corporation, 2005.

Course Title	**Internet of Things- Practical Approach using NXP Rapid**				**Course Type**		**Theory**	
Course Code	M20TL0105	**Credits**	**3**		**Class**		**I Semester**	
Internet of Things- Practical Approach using NXP Rapid	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

The transformative intersection between the Internet, mobile and sensor technology has inspired this course. Learn to create the next generation of IoT-enabling technologies, by designing an IoT system to connect embedded sensors using commodity smartphones via low power Bluetooth Low Energy. Skills such as app development and embedded system design are practiced using various applications including a sensor station. Practical exercises involving system design, device programming and cloud development is carried out using NXP rapid IoT kits.

COURSE OBJECTIVES:

The objectives of this course are:

1. To introduce the full connected-product experiences by integrating Internet services and physical objects

2. To give an insight into developing prototypes of Internet-connected products using appropriate tools
3. To introduce M2M and IoT Technology Fundamentals
4. To understand the IoT architecture and state of art

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Understand full connected-product experiences by integrating Internet services and physical objects.	1,2,3,4,5	1,2,3
CO2	Analyzing, designing, and developing prototypes of Internet-connected products using appropriate tools.	1,2,3,4,5,9,10	1,2,3
CO3	Identifying, classifying and describing different kinds of Internet-connected product concepts Describe different network protocols	1,2,3,4,9,10	1,2,3
CO4	Apply communications knowledge to facilitate transport of IoT data overvarious available communications media.	1,2,3,4, 9,10	1,2,3
CO5	Explore the state of art in IoT systems	1,2,3,4, 9,10	1,2,3
CO6	Developing the IoT system for given application using NXP Rapid IoT kit	1,2,3,4,5, 9,10	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓	✓			
CO2	✓	✓	✓			
CO3	✓	✓	✓			
CO4	✓	✓	✓			
CO5	✓	✓				
CO6				✓	✓	✓

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	1	1	1				1	3	2
CO2	3	3	3	1	1	1	2	2	2				3	2
CO3	3	3				2			1			2	3	2
CO4	3	3	1	3	2	2	3	3	3			3	3	2
CO5														

CO6														

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
OVERVIEW IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations. M2M and IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service (XaaS), M2M and IoT Analytics
UNIT - 2
REFERENCE ARCHITECTURE IoT Architecture-State of the Art – Introduction, State of the art, Reference Model and architecture, IoT reference Model - IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View. Real-World Design Constraints- Introduction, Technical Design constraints-hardware is popular again, Data representation and visualization
UNIT - 3
M2M and IoT Technology Fundamentals Device and gateways, Local and wide area networking, data management, Everything as service (Xaas), Buisiness process for IoT
UNIT - 4
Introduction, state of art: Europian Telecommunication standards institute M2M/one M2M: ETSI M2M high-level architecture, ETSI M2M service capabilities, ETSI M2M interfaces, ETSI M2M resource management **Case study:** **NXP Rapid IoT Development Kit**: Introduction, NXP rapid IoT studio, NXP MCUXpresso, architecture study.

TEXT BOOKS:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1st Edition, Academic Press, 2014.
2. Bernd Scholz-Reiter, Florian Michahelles, “Architecting the Internet of Things”, ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer
3. Daniel Minoli, “Building the Internet of Things with IPv6 and MIPv6: The EvolvingWorld of M2M Communications”, ISBN: 978-1-118-47347-4, Willy Publications
4. http://www.cse.wustl.edu/~jain/cse570-15/ftp/iot_prot/index.html
5. https://www.nxp.com/document/guide/get-started-with-the-iot-prototyping:GS-IOT-PROTOTYPING

Semester – II

Course Title	**Design of Analog CMOS Integrated Circuits**			**Course Type**	**Integrated**
Course Code	**M20TL0201**	**Credits**	**4**	**Class**	**II Semester**

	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
Design of Analog CMOS Integrated Circuits	Theory	3	3	3				
	Practice	1	2	2	Theory	Practical	**IA**	**SEE**
	Tutorial	-	-	-				
	Total	**4**	**5**	**5**	**39**	**26**	**50 %**	**50 %**

COURSE OVERVIEW:

This course focuses on transistor-level design of mixed-signal CMOS integrated circuits. After reviewing fundamentals of MOSFET operation, the course will cover design of analog building blocks such as current-mirrors, bias references, amplifiers, and comparators, leading up to the design of digitalto-analog and analog-to-digital converters. Aspects of subthreshold operation, structured design, scalability, parallelism, low power-consumption, and robustness to process variations are discussed in the context of larger systems. The course will include use of Cadence design software to explore transistor operation and to perform functional-block designs, in the process of incrementally designing a data-converter front-end.

Course Objectives:

1. To understand the basics and operation of MOS devices.
2. To analyse and understand analog CMOS integrated circuits.
3. To analyse and design single stage MOS amplifier circuits.
4. To understand the basic operation of differential amplifier and op-amps.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection	1,2,3,4,5, 9,10	1,2,3
,CO2	Design high-performance, stable operational amplifiers with the trade-offs between speed, precision and power dissipation	1,2,3,4,5, 9,10	1,2,3
CO3	Analyse the stability, feedback in amplifiers, op-amps	1,2,3,4,5,9,1 0	1,2,3
CO4	Design and study the behavior of phase-locked-loops for the applications.	1,2,3,4,5,9,1 0	1,2,3
CO5	Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance	1,2,3,9,10	1,2,3
CO6	Design ADCs and DACs, single stage, differential and current mirror.	1,2,3,4,5, 9,10	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**

CO1	✓	✓	✓	✓		
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓			
CO6					✓	

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3				3	3		1	2	2
CO2	3	2	2	2	3				3	3		1	3	2
CO3	3	1	2	3	1				3	3		3	3	2
CO4	3	3	3	1	2				1	2		3	3	2
CO5	3	2	1						2	1		2	3	1
CO6	3	2	2	2	3				2	1		1	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1 **Basic MOS Device Physics:**General considerations, MOS I/V Characteristics, second order effects, MOS device models. Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.
UNIT - 2 **Differential Amplifiers & Current Mirrors:** Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors. Operational Amplifiers: One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps.
UNIT - 3 **Oscillators and Phase Locked Loops:** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. Band gap References and Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, and Switched Capacitor Amplifiers.

UNIT - 4

Oscillators and Phase Locked Loops:DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC

PRACTICE SESSION:

Sl. No.	Name of the Practice Session	Tools and Techniques	Expected Skill /Ability
1	Design of inverter with given specifications, and perform the following • Draw the schematic and perform DC analysisTransient Analysis • Draw the Layout and perform DRC and ERC • Extract RC and Back annotate the same and verify the design	CADENCE	Design and circuit debugging. Working in a team
2	Design the following circuits with given specifications, completing the design flow mentioned below: i) A Single Stage differential amplifier ii) Common source amplifier iii) Design an opamp with given specification. • Draw the schematic and verify the following • i) DC Analysis • ii) AC Analysis • iii) Transient Analysis • Draw the Layout and verify the DRC, ERC, LVS • Extract RC and back annotate the same and verify the Design.	CADENCE	Design and circuit debugging. Working in a team

References:

1. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
2. Philip Allen and Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University, Press, 2011.
3. R. Jacaob Baker, Harry W Li and David E Boyce, “CMOS Circuit Design, Layout, Stimulation”,CMOS Circuit PHI Edn, 2005.

Course Title	Real Time Operating Systems			Course Type	Integrated
Course Code	M20TL0202	Credits	4	Class	II Semester

	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
Real Time Operating Systems	Theory	3	3	3				
	Practice	1	2	2	Theory	Practical	**IA**	**SEE**
	-	-	-	-				
	Total	**4**	**5**	**5**	**39**	**26**	**50 %**	**50 %**

COURSE OVERVIEW:

This course introduces the basics of Real-Time Operating Systems (RTOSes) using VxWorks and Linux as examples. The course focuses on the primary principles of RTOSes including determinism, real-time scheduling, interrupt latency and fast context switching as well as time and space partitioning in hard real-time environments. The first part of the course focuses on acquiring an understanding of microkernel and memory architectures for Real-Time including scheduling, signals, system calls, synchronization, inter-process communications and interrupt handling. The latter part of the course covers considerations for timing, memory management, device drivers, booting, debugging and deployment of Real-Time embedded systems.

COURSE OBJECTIVES:

1. To acquire knowledge about concepts related to OS such as Scheduling techniques,threads, inter-thread communications, and memorymanagement.
2. To acquire knowledge about different types of scheduling algorithms
3. To study about Free RTOS
4. To understand the various functions of RTOS

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Describe the fundamental concepts of RTOS	1,2,3,4,5,11	1,2,3
CO2	Develop programs for real time services, firmware and RTOS	1,2,3,4,5,6, 11	1,2
CO3	Develop programs formulate threaded applications on FreeRTOS	1,2,3,4,5,6, 11	1,2,3
CO4	Apply priority based static and dynamic real time scheduling technique forthe given specifications.	1,2,3,4,5,6, 11	1,2,3
CO5	Analyze real-rime application performance through the use of statistics	1,2,3,4	1,2,3
CO6	Analyze deadlock conditions, shared memory problem, critical sectionproblem, missed deadlines, availability, reliability and QoS.	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

	Bloom's Level

CO#	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓	✓			
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	3	1						1	1	3	2
CO2	3	3	3	3	2	1					1	2	3	1
CO3	3	3	2	3	2	1					3	3	3	2
CO4	3	3	2	3	2	1					1	3	3	1
CO5	3	3	2	3								3	3	1
CO6	2	3	1	3								3	3	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT – 1
Real time systems and Resources: Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems Requirements of Embedded System, Challengesin Embedded System. System Resources, Resource Analysis, Real-Time Service Utility. Processing with Real Time Scheduling: Scheduler Classes, Preemptive Fixed Priority Scheduling Policies with timing diagrams, Rate Monotonic least upperbound,Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies,Worst case execution time, Dead lock and live lock.
UNIT – 2
Real Time Operating Systems: Operating System basics,The Kernel and its subsystems, Kernel Space and User Space, Kernel Architecture, Types of operating system, Task, process and Threads, Multi-Processing and Multitasking, Types of multitasking, Task Scheduling, Task states, Non-Preemptive scheduling, Preemptive Scheduling,Round Robin Scheduling,IdleTask,Task Communication, Task Synchronization,Thread Safe Reentrant Functions.

UNIT – 3
Embedded Firmware Design, development and FreeRTOS: Embedded Firmware Design Approaches, Super-loop based approach, Embedded Operating System based approach, Programming in Embedded C, Integrated development environment (IDE), Overview of IDEs for Embedded System Development.
UNIT – 3
Introduction to Free RTOS, multitasking on an LPC17xx Cortex-M3 Microcontroller, LPC17xx Port of Free RTOS, Resources Used by Free RTOS, Task Management, Task Functions, Task Priorities, Idle task and task hook function, Creation and Deletion of tasks.
UNIT – 4
Embedded System design with Free RTOS Queue Management, Characteristics of Queue, Working with Large Data, Interrupt Management, Queues within an Interrupt Service Routine, Critical Sections and Suspending the Scheduler, Resource Management, Memory Management

PRACTICE SESSION:

Sl. No.	Name of the Practice Session	Tools and Techniques	Expected Skill /Ability
1	Write a C Program to perform the task Management in FreeRTOS,using win32 port on Visual Studio IDE: a. CreateTwoTasksand Pass the"Task-Name"as an argument to the task function. b. Demonstrate the useofidletaskhookfunction. c. Updatethetaskprioritydynamically.	Free RTOS, Linux	Design and program debugging. Working in a team
2	Writea C Program to create a task in FreeRTOS,using win32 porton Visual StudioIDE;that periodically generatesasoftwareinterruptforevery1sec.	Free RTOS, Linux	Design and program debugging. Working in a team
3	WWrite aC ProgramtoDemonstrate Inter-TaskCommunication using queues in FreeRTOS, useARM Cortex-M3 Port (LPC1768 MCUKit) A.Task-1createsdata(stores in a structure)andsendsitto the queue B.Task-2 readstreads thege papacket from the queue and reacts accordingly.	Free RTOS, Linux	Design and program debugging. Working in a team
4	WriteaCProgramtoDemonstrateTaskSynchronization and Resource Sharing amon g multiple tasks in Free RTOS,use ARM Cortex-M3 Port(LPC1768 MCU Kit) A. Assumemultipletasks tryingto write datatoaserialport.	Free RTOS, Linux	Design and program debugging. Working in a team

References:

1. ARM Instructor Reference Material
2. SamSiewert,"Real-Time Embedded SystemsAnd Components".
3. Shibu K.V.,"Introduction to Embedded System".
4. "Using the Free RTOS Real-time Kernel" From Free RTOS.
5. Manuals and Technical Documents from the ARMInc, web site.

Course Title	VLSI Testing				Course Type		Theory	
Course Code	M20TLS0211	Credits	3		Class		II Semester	
VLSI Testing	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	IA	SEE
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course brings an insight into concepts of VLSI Testing. Briefed profound understanding of combinational and sequential test methodologies and their applications. The knowledge of design for testability, modeling of test circuits for combinational and sequential are introduced. BIST, ATPG, LSSD basics are covered to focus on the testing methodologies.

COURSE OBJECTIVES:

The objectives of this course are:

1. Learn various types of faults and fault modeling in VLSI Systems.
2. Analyze the need for testing and testable design of digital circuits
3. Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
4. Apply the sequential circuits and memory testing methodologies such as Bourndary scan, BIST.

COURSE OUTCOMES(COs)

CO#	Course Outcomes	POs	PSOs
CO1	Understanding the need for fault modeling and testing of digital circuits	1,2,3,4	1,2,3
CO2	List the digital circuits faults and analyze the tests for efficiency	1,2,3,4, 11	1,2,3
CO3	Applying faults in digital memories and digital circuits	1,2,3,4	1,2,3
CO4	Validating the various testing methodologies withrespect to digital systems	1,2,3,4	1,2,3
CO5	Apply boundary scan technique to validate the performance of digital circuits	1,2,3,4	1,2,3
CO6	Design built-in self tests for complex digital circuits	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				

CO2	✓	✓	✓			
CO3	✓	✓	✓			
CO4	✓	✓	✓			
CO5	✓	✓	✓	✓		
CO6	✓	✓	✓	✓		

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1								1	2	1
CO2	3	3	2	1								3	2	1
CO3	2	3	2	1								3	3	2
CO4	3	2	3	1								3	3	1
CO5	2	3	3	1										
CO6	1	3	2	1										

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT – 1 **Introduction to VLSI Testing:** Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. Logic Simulation: Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation.
UNIT – 2 **Combinational Test Methdologies :** Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits.Testable Combinational logic circuit design: The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic
UNIT - 3 **Design for Testability:** Testable Combinational logic circuit design: Testable design ofmultilevel combinational circuits, Synthesis of random patterntestable combinational circuits, Path delay fault testablecombinational logic design, Testable PLA design. Test generation for Sequential circuits: Testing of sequentialcircuits as Iterative combinational circuits, state table verification,Test generation based on Circuit Structure, Functional Faultmodels, test Generation based on Functional Fault models.
UNIT - 4 **Design of testable sequential circuits and BIST :** Design of testable sequential circuits: Controllability andobservability, Ad-Hoc design rules for improving testability, design ofdiagnosable sequential circuits, the scan-path technique for testablesequential circuit design, Level Sensitive Scan Design(LSSD),Random Access Scan Technique, Partial scan, testable sequentialcircuit design using Nonscan Techniques, BoundaryScan.Test pattern generation for BIST, Outputresponse analysis, Circular BIST, BIST Architectures. Testable Memory Design: RAM Fault Models, Test algorithms forRAMs, Detection of pattern-sensitive faults, BIST techniques forRAM chips, Test generation and BIST for embedded RAMs.

TEXT BOOKS:

1. Lala Parag K., Digital Circuit Testing and Testability, New York, AcademicPress, 1997.
2. Abramovici M, Breuer M A and Friedman A D, "Digital Systems Testing andTestable Design", Wiley, 1994.

REFERENCE BOOK:

1. Vishwani D Agarwal, "Essential of Electronic Testing for Digital, Memoryand Mixed Signal Circuits", Springer, 2002.
2. Wang, Wu and Wen, "VLSI Test Principles and Architectures", MorganKaufmann, 2006.

<table>
<tr><td colspan="2">Course Title</td><td colspan="4">Semiconductor Device Modeling & Technology</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td colspan="2">Course Code</td><td>M20TLS0212</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
<tr><td rowspan="5">Semiconductor Device Modeling & Technology</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
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<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

This course introduces the concepts of semiconductor materials and their characteristics. It discusses the detailed functioning and characteristics of PN junction diode. This course also focuses on briefing the MOS structure, energy band diagram and electrical characteristics of MOSFET and FET Capacitor. It describes the working of bipolar transistor, operation modes and equivalent circuit models.

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COURSE OBJECTIVES:

The objectives of this course are:

1. Understand the basic concepts of semiconductor materials
2. Characterize the concepts of P- N Junction diode
3. Understand the basic characteristics of metal semiconductor junction
4. Study the device modeling

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Analyze the concepts of semiconductor materials , P-N Junction Diode and analyze its characteristics	1,2,3,4	1,2,3
CO2	Compute carrier electronic properties in semiconductor materials and devices under different operating conditions.	1,2,3,4	1,2
CO3	Analyze the characteristics and concepts of MOSFET and BJT and draw band diagram of different semiconductor devices under different bias conditions	1,2,3,4	1,2
CO4	Apply, Awareness and Understanding of current trends in semiconductor device modeling in Design and Fabrication Unit	1,2,3,4	1,2

CO5	Analyze working principle and characteristics of FET.	1,2,3,4	1,2
CO6	Design the digital circuits using various logic gates	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓				
CO3	✓	✓	✓	✓		
CO4	✓		✓			
CO5	✓	✓	✓	✓		
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2								1	2	1
CO2	3	2	1	3								3	2	
CO3	3	3	2	3								3	3	
CO4	3	3	2	2								3	3	
CO5	3	3	1	2								3	3	
CO6	3	3	2	2								3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
Semiconductor Materials : Intrinsic carrier concentration: Dopant atoms and energy levels, Ionization energy: the extrinsic semiconductor, Position of Fermi-energy level, variation of EF with doping concentration and temperature. Carrier drift: mobility, conductivity and velocity saturation, Carrier Diffusion: diffusion current density, total current density, The Einstein relation, Excess carrier generation and recombination, Characteristics of excess carriers – continuity equation and time-dependent
UNIT - 2
PN Junction diode: Basic structure, built-in potential, electric field, space charge width, reverse applied bias space charge width and Electric field, junction capacitance, Ideal current-voltage relationship, minority carrier distribution, Ideal PN-junction currents under forward and reverse bias, Temperature effects, small signal model of PN-junction, Equivalent circuits, recombination current, junction breakdown; SPICE models of p-n diode.

UNIT - 3
Metal Semiconductor Junction and FET Capacitor: Schottky barrier, I-V and C-V characteristics of M-S junction, thermal emission and tunneling current, Field-Effect Transistors: JFET- current-voltage characteristics, effects in real devices, high-frequency and high-speed issues. MOS structure: Energy band diagrams, work function difference, Depletion layer thickness, Flat band voltage, threshold voltage, charge distribution, MOS Capacitance – voltage characteristics.
UNIT - 4
Bipolar Transistor and Current trends: Basic Principle of Operation: Simplified transistor current relationship, Modes of operation amplification with bipolar transistors, Minority carrier distribution, Forward active mode and other modes of operation, Lov frequency common base current gain, Non-ideal effects – Base width modulation, breakdown voltage, equivalent circuit models Eber's – Moll model, Hybrid – pi model, Frequency limitation, large signal switching; SPICE models of BJT.

REFERENCE BOOK:

1.N. Das Gupta, and A. DasGupta, Semiconductor Devices: Modelling and Technology, Prentice Hall of India Private Limited, New Delhi, 2004.

2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 5th edition, Prentice Hall of India Private Limited, New Delhi, 2000.

3.. Chenming Calvin Hu, Modern Semiconductor Devices for Integrated Circuits, Pearson, 2009.

4. Y. Taur, and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University press, 1998

5. S. M. Sze, **"VLSI Technology**", 2nd edition, McGraw-Hill, 1998

6. S. K. Dieter, **"Semiconductor Material and Device Characterization,"** by John Wiley and Sons, New York, 1990.

7. G. W. Roberts and A. S. Sedra SPICE 2nd edition, Oxford University Press, 1997

8. Yuan TaurandTak H. Ning, **"Fundamentals of Modern VLSI Devices",** Cambridge University Press; 2 edition, 2013.

Course Title	**IC Fabrication**				**Course Type**		**Theory**	
Course Code	**M20TLS0213**	**Credits**	**3**		**Class**		**II Semester**	
IC Fabrication	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

The course provides an overview of the foundations of microelectronic fabrication technology, which entered into the Nanotechnology Era around the year 2000 consistent with Moore's Law. The success of microelectronic fabrication technology relies on continuous improvement of integrated circuit performance. This continuous need for device scaling is summarized in Moore's Law which postulates that the level of chip complexity that can be manufactured for minimal cost is an exponential function that doubles in a period of time. The various concepts such as etching, implantation, metallization and process integration are discussed

COURSE OBJECTIVES:

The objectives of this course are:

1. To introduce the IC fabrication concepts
2. To give an insight into environment for fabrication of VLSI technology

3. To know various steps involved in VLSI fabrication.
4. To make aware of various IC technologies and packaging of VLSIdevices.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Understand the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication.	1,2,3,4	1,2,3
CO2	Know the different IC technologies and fabrication.	1,2,3,4	1,2,3
CO3	Analyzing the VLSI device packaging and design considerations	1,2,3,4	1,2,3
CO4	Eploring the metalization techniques in Fabrication process	1,2,3,4	1,2,3
CO5	Illustrate VLSI process integration techniques	1,2,3,4	1,2,3
CO6	Know the state of art in IC fabrication	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓				
CO3	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2								1	2	1
CO2	1	3	3	2								3	2	1
CO3	1	3	2	3								3	3	2
CO4	2	1	3	1								1	2	3
CO5	2	2	1	3								2	3	1
CO6	3	2	3	1								1	2	3

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents

UNIT - 1
Environment for VLSI Technology : Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques. Electronic-Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Process Considerations Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation. Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Optical contrast,contrastcurve, MTF.
UNIT - 2
Etching: Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes,P-well,N-well,twin-well process
UNIT - 3
Implantation Technique: Ion Implantation:Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation, isolation methods-PN junction, Trench isolation,ohmic contacts
UNIT - 4
Metalization and VLSI process Integration: Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization Problems, New Role of Metallization, Testing of VLSI circuits **VLSI Process Integration:** Introduction, Fundamental Considerations for IC Processing, , CMOS IC Technology,, Bipolar IC Technology, IC Fabrication, Stick diagram-rules for stick diagram, design rules Packaging of VLSI Devices: Introduction, Package Types, Packaging Design Considerations

REFERENCE BOOK:

1. S. M. Sze, “VLSI Technology”, McGraw-Hill, Second Edition.
2. S.K. Ghandhi, "VLSI Fabrication Principles", John Wiley Inc., New York, 1994, Second Edition.
3. S.A. Campbell, “The Science and Engineering of Microelectronic Fabrication”, Oxford University Press, 2nd edition, 2001

Course Title	**ASIC Design**				**Course Type**		**Theory**	
Course Code	**M20TLS0214**	**Credits**	**3**		**Class**		**II Semester**	
ASIC Design	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	**IA**	**SEE**
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course allows the student to be an entry-level industrial standard ASIC or FPGA designer. It gives an understanding of the ASIC/FPGA design and implementation related issues and tools. The course aims at providing an understanding of basics Chip-based system and Platform design

COURSE OBJECTIVES:

The objectives of this course are:

1. Explain ASIC methodologies and programmable logic cells to implement a functionon IC.

2. Analyse back-end physical design flow, including partitioning, floor-planning,placement, and routing.
3. Understand the ASIC Cell library design
4. Knowledge to carry out FPGA and ASIC designs.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Describe the concepts of ASIC and FPGTA design methodology.	1,2,3,4	1,2,3
CO2	Analyze the data path elements and netlist and calculate the logical effort of the VLSI circuits.	1,2,3,4	1,2,3
CO3	Design VLSI systems targeted to FPGAs and ASICs for specific application and perform design entry, physical design flow.	1,2,3,4	1,2,3
CO4	Explore the logic synthesis process of digital circuits	1,2,3,4	1,2,3
CO5	Illustrate the programmable ASIC technology	1,2,3,4	1,2,3
CO6	Create floor plan including partition and routing with the use of CAD algorithms.	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓				
CO3	✓	✓	✓			
CO4	✓	✓	✓			
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2								1	2	1
CO2	3	2	3	1								3	2	1
CO3	1	3	2	3								3	3	2
CO4	3	3	1	2								3	1	2
CO5	1	3	2	3								2	3	1
CO6	1	3	2	3								2	3	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT – 1 **Introduction to ASIC** Introduction to ASICs: Full custom, Semi-custom and ProgrammableASICs, ASIC Design flow, ASIC cell libraries.CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carryskip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier(Booth encoding), Data path Operators, I/O cells, Cell Compilers.Transistors as Resistors – Transistor Parasitic Capacitance, Logical effort -Library cell design, Library architecture. Optimum delay and number of stages.
UNIT – 2 **Unit 2:Programmable Asics– Programmable Asic Logic Cells And Programmable Asic I/O Cells** Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT – Xilinx LCA –Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock & Power inputs – Xilinx I/O blocks.
UNIT – 3 **Logic Synthesis, Simulation And Testing** Verilog and logic synthesis –VHDL and logic synthesis – types of simulation –boundary scan test – fault simulation – automatic test pattern generation
UNIT – 4 **Floor Planning and Placement** **Floor planning** Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clockplanning.**Placement**: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, PhysicalDesign Flow

Reference Books:

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison- Wesley Professional; 2005.
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.

<table>
<tr><td>Course Title</td><td colspan="4">Static Timing Analysis</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td>Course Code</td><td>M20TLS0215</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
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<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

In this course, the student shall learn the basic concepts of static timing analysis and apply them to constrain a design. Also the student shall apply these concepts to set constraints, calculate slack values for different path types, identify timing problems, and analyze reports generated by static timing analysis tools.

COURSE OBJECTIVES:

The objectives of this course are:

1. Understand the basic concepts of timing analysis, signal integrity at the various processes, environments and interconnect corners.

2. Apply the concepts of Static timing analysis to evaluate the delay of the digital systems.
3. Generating the various timing analysis report using EDA tool.
4. Set up and hold timing analysis for digital systems.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Evaluate the delay of any given digital circuits.	1,2,3,4	1,2,3
CO2	Perform the static timing analysis by applying constraints and generating the appropriate reports using EDA tool	1,2,3,4	1,2,3
CO3	Identify critical paths and timing violations.	1,2,3,4	1,2,3
CO4	Applying appropriative techniques to meet the timing of the design.	1,2,3,4	1,2,3
CO5	Generate the timing analysis report for different checks.	1,2,3,4	1,2,3
CO6	Perform verification and analyze the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓	✓			
CO2	✓	✓	✓			
CO3	✓	✓	✓			
CO4	✓	✓	✓			
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	3								2	1	3
CO2	3	2	1	2								2	1	3
CO3	3	1	2	3								3	2	3
CO4	2	3	1	2								3	2	3
CO5	3	1	2	3								3	2	3
CO6	3	1	2	3								3	2	3

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT – 1
Introduction: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk and Noise, Design Flow CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis Power Considerations, Reliability Considerations, STA Concepts: CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions .
UNIT – 2
Standard Cell Library Standard Cell Library: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, Timing Models - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setup and Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State-Dependent Models XOR, XNOR and Sequential Cells, Interface Timing Model for a Black Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage,, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and Sequential Cells, Other Noise Models, Power Dissipation Modeling, Active Power, Double Counting Clock Pin Power, Leakage Power, Other Attributes in Cell Library, Area Specification, Function Specification, SDF Condition, Characterization and Operating Conditions, What is the Process Variable, Derating using K-factors, Library Units.
UNIT – 3
Interconnect Parasitics Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation of Extracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets. Delay Calculation: Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation.
UNIT – 4
STA Environment and Path Segmentation Configuring the STA Environment: What is the STA Environment? Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge_shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example C, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Specifying Inactive Signals, Breaking Timing Arcs in Cells, Point-to-Point **Specification, Path Segmentation:** Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input

REFERENCE BOOK:

1. 1 J. Bhasker, R Chadha, “Static Timing Analysis for Nanometer Designs: A Practical Approach”, Springer, 2009.
2. Sridhar Gangadharan, Sanjay Churiwala, “Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)”, Springer, 2013.
3. Naresh Maheshwari and SachinSapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999.

Course Title	Unix/Linux Shell Scripting and Python Basics				Course Type		Theory	
Course Code	M20TLS0221	Credits	3		Class		II Semester	
Unix/Linux Shell Scripting and Python Basics	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	IA	SEE
	-	-	-	1 -				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

In this course student will be introduced to the Unix Operating System, its various features, basic and advanced levels of Unix and Shell scripting techniques. Students will get to know about the architecture of Unix, its various commands and the Unix Server.The course also enables python coding to be learned and has a great knowledge of the python programming language

COURSE OBJECTIVES:

The objectives of this course are:

1. Understand and write the shell scripts
2. Understand the concept of process in Unix
3. Study the basic concepts of python scripting language

COURSE OUTCOMES(COs)

CO#	Course Outcomes	POs	PSOs
CO1	Design scripting code for a given application	1,2,3,4,5	1,2,3
CO2	Make use of language constructs to solve real world problems using shell scripting	1,2,3,4,5	1,2,3
CO3	Develop programs for text processing and other application domains by making use of regular expressions.	1,2,3,4,5	1,2,3
CO4	Apply various conditional statements, loops and command line arguments to develop the script code	1,2,3,4,5	1,2,3
CO5	Develop the python scripting code for given application	1,2,3,4,5	1,2,3
CO6	Recognize the need and engage in learning new libraries and tools in linux/unix shell scripting.	1,2,3,4,5	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

	Bloom's Level

CO#	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓	✓			
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓	✓	✓	
CO6	✓	✓	✓	✓	✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2	1							1	2	1
CO2	3	3	3	2	1							3	2	1
CO3	3	3	2	3	1							3	3	2
CO4	2	3	3	3	2							3	3	1
CO5	2	3	1	3	2							2	3	1
CO6	1	2	3	3	1							3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents

UNIT – 1

Shell Basics, Writing first script Types of shells, Shell functionality, Environment, Writing script & executing basic script, Debugging script, Making interactive scripts, Variables (default variables), Mathematical expressions,

Conditional Statements and Loops: If-else-elif, Test command, Logical operators-AND,OR,NOT, ase –esac, Loops, While, For, Until, Break & continue

UNIT – 2

Command line arguments

Positional parameters, Set & shift, IFS, Break & continue, Processing file line by line Functions, What is regular expression, Grep, cut, sort commands, Grep patterns.

UNIT – 3

SED& AWK, Processes

Concept of process in Unix, Background processes, Scheduling processes -At, batch &Cron

UNIT – 4

Python Basic

Latest developments in the semiconductor device modeling and introduction to device simulation tools & technologies, e.g., Silvaco-CMOS Process and Smart SPICE. Exposure to equipment and process used in Semiconductor Fab. Unit, Test and Measure Equipments.

Reference Books:

1. Brian W. Kernighan & Rob Pike, The Unix Programming Environment, Prentice Hall of India Private Limited, New Delhi, 2004.
2. Carl Albing, JP Vossen, and Cameron Newham,BashCookbook,O'Reilly 2007.
3. Tim Hall and J-P Stacey,Python for Absolute Beginners, Apress, 2009.

<table>
<tr><td>Course Title</td><td colspan="4">SOC Design</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td>Course Code</td><td>M20TLS0222</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
<tr><td rowspan="5">SOC Design</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

This course discusses the SoC architecture princples and components threof. The processor selection knowledge and power, area, time trade off in system design. The processor architectures and their working principles will be introduced to students as well. The Network On Chip basics will be discussed. This provides and overview of the problems relevant to ASIC/FPGA design/ implementation and tools. The course aims at providing an understanding of basics Chip-based system and Platform design.

COURSE OBJECTIVES:

The objectives of this course are:

1. Provide a comprehensive introduction to the ASIC and SoC technology.
2. Provide theoretical and practical aspects of ASIC and SoC design.
3. Introduce ASIC design, ASIC library design and Programmable ASIC.
4. Give an overview to SoC design, its challenges and Design flow.
5. To understand the memory design concepts in processors.
6. To understand ASIC design flow using semi/full /standard cells.

Mapping of Course Outcomes with programme Outcomes

CO#	Course Outcomes	POs	PSOs
CO1	Select the appropriate processors for a given application keeping area, power and speed as constraints and to Deepen CMOS VLSI design knowledge.	1,2,3,4	1,2,3
CO2	Explore the network on chip technologies and list the advantages and bottlenecks of different No topologies.	1,2,3,4	1,2,3
CO3	Analyze the performance of memories using reconfigurable architectures for rapid prototyping.	1,2,3,4	1,2,3

CO4	Describe the ASIC Design methodology and summarize ASCI cell library design	1,2,3,4	1,2,3
CO5	Use the concepts and methodologies employed in designing a System- on-chip (SoC) base around a microprocessor core and in designing the microprocessor core itself.	1,2,3,4	1,2,3
CO6	Analyze the requirements of a modern operating system and use the architecture to address the same.	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓				
CO3	✓	✓				
CO4	✓	✓	✓			
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2								1	2	1
CO2	3	3	3	3								3	2	1
CO3	3	3	2	2								3	3	2
CO4	3	3	1	2								3	3	2
CO5	2	2	3	1								1	3	2
CO6	3	1	2	1								2	2	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
System Approach and Chip Basics System Architecture, Components of the System, Hardware and Software. An approach for SoC Design, System On Chip Design Process: A canonical SoC Design, SoC Design flow - waterfall vs spiral, Top-down vs Bottom up, System Architecture and Complexity. Chip Basics. Cycle Time, Die Area and Cost, Ideal and Practical Scaling, Power, Area–Time–Power Trade-Offs in Processor Design, Reliability, Configurability.

UNIT - 2
Processors and Interconnects Processor Selection for SoC, Basic Concepts in Processor Architecture, Instruction Handling, and Buffers, Minimizing Pipeline Delays, Branches. Vector, Very Long Instruction Word (VLIW), and Superscalar with case studies. Interconnect architectures for SoC. Bus architecture. Network on Chip topologies. Routing, Switching and Flow Control in NoCs.
Memory Design System-on-Chip and Board-Based Systems – Scratchpads and Cache Memory, Basic Notions, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Cache, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SoC (On-Die) Memory Systems, Board-based (Off-Die) Memory Systems, Simple DRAM and the Memory Array, Models of Simple Processor–Memory Interaction.
ASIC Design Full/Semi Custom with ASIC, Standard Cell based ASIC, Gate array based ASIC, Programmable logic device, FPGA design flow, ASIC cell libraries. ASIC Library Design, Logical effort and library cell design. Low-Level Design Entry, Schematic Entry, Hierarchical design, the cell library, connections, vectored instances and buses, Edit in place attributes, Net list, screener, back annotation.

Reference Books:

1. Micheal J Flynn and Wayne Luk,"**Computer System Design: System-on-Chip**," Wiley, First Edition, 2011.
2. Sudeep Pasricha and NikilDutt,"**On-Chip Communication Architectures: System on Chip Interconnect**", Morgan Kaufmann, 2008.
3. Michael Keating, Pierre Bricaud, "**Reuse Methodology manual for System on chip designs**", Kluwer academic Publishers, 2nd edition-2008.
4. M.J.S .Smith, "**Application Specific Integrated Circuits**", Pearson Education, 2003.

Reference Books:

1. Rao R. Tummala, MadhavanSwaminathan, "**Introduction to system on package sop-Miniaturization of the Entire System**", McGraw-Hill-2008.
2. James K. Peckol, "**Embedded Systems: A Contemporary Design Tool**", WILEY Student Edition, 2007.
3. Ahmed Amine Jeraya, Wayne Wolf, "**Multiprocessor System On chip**", Morgan Kauffmann, 2005.

<table>
<tr><td colspan="2">Course Title</td><td colspan="4">Embedded Systems For Automotive Applications</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td colspan="2">Course Code</td><td>M20TLS0223</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
<tr><td rowspan="5">Embedded Systems For Automotive Applications</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

Today's modern vehicle equipped with networked measurement, control and communications systems to meet the growing demands for complex features, including increased safety (brake systems, airbag system, Electronic Stability Program - ESP), driver assistance systems (cruise control, navigation, night vision, blind spot detection)

or to comply with legal requirements (reducing the emission of pollutants by intelligent engine control).On-board diagnostics (OBD) check the operation of almost every electrical / electronic part in every major vehicle system. The objective of the course is to provide understanding of the techniques essential to the design and implementation of embedded systems using suitable hardware and software tools for Automotive Application. This course offers a range of topics of immediate relevance to industry and makes the participants exactly suitable for Automotive Industry.

COURSE OBJECTIVES:

The objectives of this course are:

1. Provide a comprehensive introduction to Automative fundamentals
2. Describing thevarious systems in power train electronics and body of electronic systems.
3. Understanding the concepts of electric/hybrid vehicless and their configurations.

Mapping of Course Outcomes with programme Outcomes

CO#	Course Outcomes	POs	PSOs
CO1	Know the various parts of power train electronics, the body of electronic systems and hybrid vehicles	1,2,3,5,7,8,9,10,11	1,2,3
CO2	Analyze the body electronics systems	1,2,3,4,8	1,2,3
CO3	Comprehensive analysis of electric/hybrid vehicles and their configurations.	1,2,3,5,9	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓		✓		
CO3	✓	✓			✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1		2		3	1	3	1	1	1	2	1
CO2	3	3	3	2				1				3	2	1
CO3	3	3	2		1				2			3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT - 1
Automotive Fundamentals – Vehicle functional domains and requirements, The systems approach to control and automotive instrumentation, Sensors and actuators in various vehicle domains.

UNIT - 2
Unit 2: Systems in Power Train electronis Systems in Power train Electronics: Engine Management Systems: Spark Ignition, Petrol/ Diesel Injection Systems, Transmission Systems. Systems in Chassis control: ABS, ESP,TCS, Active Suspension Systems, Cruise control and adaptive cruise control systems – Drive-by wire systems.
UNIT - 3
Unit 3: Body Electronic Systems Body electronic systems: Power Generation/ Storage, starting motor systems, Vehicle wiring systems, HVAC, Automotive alarm systems, Vehicle immobilization &deactivation, Driver information systems, Parking systems, Central locking system – electric windows – Occupants and driver safety systems: Seat belt lighteners and air-bags Diagnostics Systems.
UNIT - 4
Unit 4: Electric/Hybrid Vehicles and their configurations Electric/Hybrid Vehicles and their configurations – Autonomous Vehicles and their challenges. Introduction to Embedded automotive protocols: LIN, CAN,FlexRay, MOST - AUTOSAR standard and its applications – OSEK/VDX Open Systems in Automotive Networks.

References Books:

1. William B. Ribbens, "Understanding Automotive Electronics - An Engineering Perspective",Eight Edition, Elsevier Inc., 2017.
2. V. A. W. Hillier and David R. Rogers, "Hillier's Fundamentals of Motor Vehicle Technology on Chassis and Body Electronics", Fifth Edition, Nelson Thrones, 2007.
3. Robert Bosch GmbH, "Bosch Automotive Electricsand Automotive Electronics - Systems and Components,Networking and Hybrid Drive", Fifth Edition, Springer Vieweg, 2007.
4. Joseph Lemieux, "Programming in the OSEK/VDX Environment", CMP Books, USA, 2001.
5. Tom Denton, "Automobile Electrical and Electronic Systems", Third Edition, Elsevier Butterworth-Heinemann, 2004.

<table>
<tr><td>Course Title</td><td colspan="4">Advanced Computer Architecture</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td>Course Code</td><td>M20TLS0224</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
<tr><td rowspan="5">Advanced Computer Architecture</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

This course provides an overview of computer architecture, which stresses the underlying design principles and the impact of these principles on computer performance. General topics include design methodology, processor design, control design, memory organization, system organization, and parallel processing are discussed.

COURSE OBJECTIVES:

The objectives of this course are:

1. Interpret the quantitative principles of computer design and their performance.

2. Schedule the concepts of instruction level parallelism.
3. Apply the fundamentals of advanced memory hierarchy.
4. Illustrate the basics of VLIW processors.
5. Interpret the concepts of multiprocessors and inter process communication.

COURSE OUTCOMES(COs)

CO#	Course Outcomes	POs	PSOs
CO1	Illustrate the importance of power and performance for given computer architecture.	1,2,3,4, 5	1,2,3
CO2	Distinguish the pitfalls and fallacies for the performance in the computer architecture	1,2,3,4, 5	1,2,3
CO3	Summarize the instruction level parallelism and its importance with respect to performance and power dissipation in computer architecture.	1,2,3,4, 5	1,2,3
CO4	Differentiate the efficient hardware and software for the VLIW processors.	1,2,3,4, 5	1,2,3
CO5	Learn the advanced processor architectures for suitable applications	1,2,3,4, 5	1,2,3
CO6	Apply pipelining concept for the performance evaluation	1,2,3,4, 5	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓			✓	
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓				
CO5	✓	✓				
CO6	✓	✓			✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	1	1	3							1	2	1
CO2	3	3	3	2	2							3	2	1
CO3	3	3	2	1	2							3	3	2
CO4	3	2	1	3	3							3	3	1

CO5	2	1	3	2	1							2	3	1
CO6	3	2	2	1	3							3	2	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
Unit 1: Introduction and Review of Fundamentals of Computer Design Introduction; Classes computers, Defining computer architecture, Trends in Technology, Trends in power in Integrated Circuits, Trends in cost, Dependability, Measuring, reporting and summarizing Performance, Quantitative Principles of computer design, Performance and Price-Performance; Fallacies and pitfalls; Case studies. Some topics in Pipelining, Instruction –Level Parallelism, Its Exploitation and Limits on ILP: Introduction to pipelining,
UNIT - 2
Unit 2: Memory Hierarchy Design, Storage Systems Review of basic concepts, Cross cutting issues in the design of memory hierarchies, Case study of AMD Opteron memory hierarchy, Fallacies and pitfalls in the design of memory hierarchies, Introduction to Storage Systems, Advanced topics in disk storage. Case study of NetAA FAS6000 filer; Fallacies and pitfalls.
UNIT - 3
Unit 3: Hardware and Software for VLIW and EPIC Introduction Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism, Hardware Support for Exposing Parallelism: Predicated Instructions, Hardware Support for Compiler Speculation, The Intel IA-64 Architecture and Itanium Processor, Concluding Remarks.
UNIT - 4
Unit 4: Large-Scale Multiprocessors and Scientific Applications Introduction, Interprocessor Communication The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications, Implementing Cache Coherence

Reference Books:

1. Hennessey and Patterson, "**Computer Architecture A Quantitative Approach**", 4th Edition, Elsevier, 2007.
2. Kai Hwang, "**Advanced Computer Architecture - Parallelism, Scalability, Programmability**", 2nd Edition, 1992.

Course Title	**Designing with Power Devices**				**Course Type**	**Theory**
Course Code	**M20TLS0225**	**Credits**	**3**		**Class**	**II Semester**
	TLP	Credits	Contact Hours	Work Load	Total Number of Classes	Assessment in

Designing with Power Devices	Theory	3	3	3	Per Semester		Weightage	
	Practice	-	-	-	Theory	Practical	**IA**	**SEE**
	-	-	-	-				
	Total	3	3	3	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

The aim of this course is that the students should develop and demonstrate an enhanced knowledge regarding power electronic components as well as the design and applications of power electronic converters. In the area of components it is particularly the semiconductors for power electronics that are studied. The aim is to highlight their properties from a power electronic perspective and how these affect the converter design. In the field of applications different applications of power electronic equipment connected to the grid are studied, such as , FACTS equipment, power factor correctors, UPS and power conditioners.

COURSE OBJECTIVES:

1. To know the different power semiconductor device used for high voltage electrical applications
2. Understand the characteristics of various power devices.
3. Design of the transformer, coils and SMPS for given specification
4. Learn the idea to design the UPS and power supplies

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Know the working various power devices and characterize the electrical parameters	1,2,3	1,2,3
CO2	Exploring the various architectures of SMPS module	1,2,3	1,2
CO3	Illustrate the working of coils and windings.	1,2,3,4	1,2
CO4	Demonstrate the usage of ICs in power systems	1,2,3,4	1,2
CO5	Analyzing the working of UPS	1,2,3,4	1,2
CO6	Study the state of art in power supply units	1,2,3,4	1,2

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓			✓		
CO3	✓				✓	
CO4	✓	✓				

CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2								1	2	1
CO2	3	3	3	2								3	2	
CO3	3	3	2	1								3	3	
CO4	2	3	1	3								3	2	
CO5	3	3	2	1								2	2	
CO6	1	2	2	1								3	2	

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT – 1
Unit 1:Power Semiconductor Devices General characteristics of Power devices such as GTOs, Power BJT ,Power MOSFET,IGBT, MCT.
UNIT - 2
Unit 2: Transformer Design Fundamentals, Selection of core material, Insulating material and wires, Design Methodology of pulse transformers, High Frequency transformers, Design of Transformers for PWM converters
UNIT - 3
Unit 3: Coils and Switch Mode Power Supplies Fundamentals, Selection of core material, Insulating materials and wires, Design of inductors for power frequency, Radio frequency & High frequency Basic regulators-Buck,Boost, Buck Boost, Derived topologies-flyback, forward, Pushpull, half & full bridge converter, Special converters like Cuk" converter, PWM control techniques, Study of PWM control ICs Design of base derive circuits, Design of input section, output section & control section, Thermal design concepts, EMI/EMC considerations, Protection circuit design for power supplies.
UNIT - 4
UPS and Other Power Supplies Concept of Uninterrupted power supplies, Inverter preferred (online UPS), Line preferred UPS system (offline UPS system), Line interactive UPS system, Reliability of UPS system, Solar cells as power source devices & their characteristics.

Reference Books:

1. George Chryssis, High frequency switching power supplies: theory & design" McGraw Hill Book Co. 1984
2. K.Kitsum, " Switch mode power conversion –basic theory and design" Marcel Deckker Inc, 1984
3. N.Radhakrishnan and S.R.Bhat, "Design and technology of low power transformers and inductors" CEDT, July 1998

Course Title	Nanoelectronics				Course Type		Theory	
Course Code	M20TLS0231	Credits	3		Class		II Semester	
Nanoelectronics	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	IA	SEE
	-	-	-	-				
	Total	3	3	3	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

Traditionally, progress in electronics has been driven by miniaturization. But as electronic devices approach the molecular scale, classical models for device behavior must be abandoned. Approaching the molecular scale, traditional system behavior models have to be abandoned. This course focuses on the theory of current, voltage and resistance from atoms up. Principle of quantum mechanics is introduced to describe electrons at the nanoscale.The concepts of inorganic semiconductor nanostructure and fabrication techniques are also introduced.

.

COURSE OBJECTIVES:

1. Enhance basic engineering science and technological knowledge of nanoelectronics
2. Explain basics of top-down and bottom-up fabrication process, devices and systems.
3. Describe technologies involved in modern day electronic devices.
4. Appreciate the complexities in scaling down the electronic devices in the future.

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COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Know the principles behind Nanoscience engineering and Nanoelectronics.	1,2,3,4	1,2,3
CO2	Apply the knowledge to prepare and characterize nanomaterials.	1,2,3,4	1,2,3
CO3	Know the effect of particles size on mechanical, thermal, optical and electricalproperties of nanomaterials.	1,2,3,4	1,2,3
CO4	Illustrate the process flow required to fabricate state of the art transistor technology and explore the requirements for new materials, device structure in the future technologies.	1,2,3,4	1,2,3

CO5	Design the process flow required to fabricate state of the art transistor technology.	1,2,3,4	1,2,3
CO6	Know the state of art in trends in nano electronics	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓				
CO3	✓	✓				
CO4	✓	✓				
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2								1	2	1
CO2	1	2	3	3								3	2	1
CO3	3	3	2	3								3	3	2
CO4	3	3	1	1								3	3	2
CO5	3	3	1	1								1	2	3
CO6	2	1	3	1								2	3	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT 1
Nanoscience and Engineering Nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems
UNIT – 2
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties

UNIT - 3

Inorganic semiconductor nanostructures Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states. Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes

UNIT - 4

Fabrication techniques Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS

Reference Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.
3. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

Course Title	**VLSI for Signal Processing**				**Course Type**		**Theory**	
Course Code	**M20TLS0232**	**Credits**	**3**		**Class**		**II Semester**	
VLSI for Signal Processing	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

Digital signal processing (DSP) has emerged over last two decades as the single most key component in all electronic applications, e.g., multimedia and mobile communications, video compression, digital still and network cameras, mobile phones, radar imaging, acoustic beamformers, GPS, biomedical signal processing etc. Most of these applications impose several challenges in the implementation of DSP systems, like capability to process high throughput data as demanded by the real time application, as well as requiring less power and less chip area.This course aims at providing a comprehensive coverage of some of the important techniques for designing efficient VLSI architectures for DSP. Towards this, architectural optimization at various levels will be considered. The course assumes minimal prerequisites - an undergraduate level knowledge of digital circuit design and elementary DSP operations is sufficient for one to be able to attend the course. Apart from regular students, participants from academia may thus find the course to be useful to develop similar courses at their respective institutions.

COURSE OBJECTIVES:

1. To understand the basic concepts of DSP algorithms.
2. To analyze the various pipelining and parallel processing techniques.
3. To analyze the retiming and unfolding algorithms for various DSP applications.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Apply DSP algorithms on to the IC technology.	1,2,3,4	1,2,3
CO2	Analyze the concept of pipelining and other processing for DSP applications.	1,2,3,4	1,2,3
CO3	Optimize the area and performance of DSP applications targeted to VLSI platform.	1,2,3,4	1,2,3
CO4	Illustrate the DSP algorithms using block diagrams, signal flow graphs and data-flow graphs	1,2,3,4	
CO5	Exploiting parallel architecture of signal processing applications	1,2,3,4	
CO6	Develop an algorithm or architecture or circuit design for DSP applications	1,2,3,4,5	

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓		✓		
CO3	✓	✓		✓	✓	
CO4	✓	✓				
CO5	✓	✓				
CO6	✓	✓		✓	✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	3								1	2	1
CO2	3	1	2	2								3	2	1
CO3	3	3	2	3								3	3	2
CO4	1	2	3	1								1	2	1
CO5	2	2	3	1								3	2	1

CO6	3	2	3	1	2							3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents

UNIT - 1

Introduction to DSP systems Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DS Algorithms.

Iteration Bounds:Data flow graph Representations, loop bound and Iteration bound, Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

Pipelining and parallel processing, pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

UNIT - 2

RetimingDefinition and Properties, Solving Systems of Inequalities, Retiming Techniques, Unfolding an Algorithm for Unfolding, Properties of Unfolding, and Critical path, Unfolding and Retiming, Application of Unfolding.

Systolic architecture design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays**.**

UNIT - 3

Fast convolution Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic Convolution Design of fast convolution Algorithmby Inspection.

UNIT - 4

Pipelined and Parallel recursive and adaptive filter Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order II digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Usin Pipe lining and parallel processing, pipelined Adaptive digital filter.

References Books:

1. KeshabK.Parthi, "**VLSI Digital Signal Processing systems, Design and Implementation**", Wiley, Inter Science, 1999.
2. Mohammed Isamail and Terri Fiez, "**Analog VLSI Signal and Information Processing**", Mc Graw-Hill, 1994.
3. S.Y. Kung, H.J. White House, T. Kailath, "**VLSI and Modern Signal Processing**", Prentice Hall, 1985.
4. Jose E. France, YannisTsividis, "**Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing**", Prentice Hall, 1994.

Course Title	**Low Power VLSI Design**				**Course Type**	**Theory**
Course Code	**M20TLS0233**	**Credits**	**3**		**Class**	**II Semester**
Low Power VLSI Design	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester	Assessment in Weightage
	Theory	3	3	3		

Practice	-	-	-				
-	-	-	-	Theory	Practical	**IA**	**SEE**
Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course deals with issues and models to design low-power VLSI circuits, fundamentals of power dissipation in microelectronic devices, will be able to estimate power dissipation due to switching, short circuit. The architectural, algorithm power estimation and optimization techniques will be discussed.

COURSE OBJECTIVES:

This course will enable students to:

1. Understand different sources of power dissipation in CMOS.
2. Explore the various low power simulation techniques.
3. Focus on synthesis of different level low power transforms.

Analyze the various power techniques using different levels of design abstraction.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Analyze different sources of power dissipation and the factors involved in VLSI Systems.	1,2,3,4,5	1,2,3
CO2	Apply various available simulation techniques to estimate power dissipation in digital circuits.	1,2,3,4,5	1,2,3
CO3	Illustrate the impact of various low powers transform on power dissipation.	1,2,3,4,5	1,2,3
CO4	Interpret the real-world low power design techniques at different levels of design abstraction.	1,2,3,4,5	1,2,3
CO5	Demonstrate the power dissipation analysis, estimation and optimization techniques at architectural level	1,2,3,4,5	1,2,3
CO6	Use optimization and trade-off techniques that involve power dissipation of VLSI systems	1,2,3,4,5	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓	✓	✓		
CO5	✓	✓	✓	✓	✓	
CO6	✓	✓	✓	✓	✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	2	1							1	2	1
CO2	3	1	3	2	3							3	2	1
CO3	3	3	2	2	3							3	3	2
CO4	3	3	2	3	1							3	3	1
CO5	3	1	3	2	3							1	2	1
CO6	3	3	2	2	3							3	2	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
IntroductionNeed for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Impact of technology Scaling, Technology.
UNIT – 2
Power estimation, Simulation Power analysisSPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.
UNIT - 3
Synthesis for low power and Low power Clock distribution Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, **Clock distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.
UNIT - 4
Algorithm and Architectural Level Power Analysis and Optimization Algorithm & Architectural Level Methodologies: Introduction, design flow Algorithmic level analysis & optimization, Architectural level estimation & synthesis. **Software design for Low power:** Introduction, sources of software power dissipation, software power estimation, software power optimization- minimizing the memory access costs.

References Books:

1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000.
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002.
3. Rabaey, Pedram, "**Low Power Design Methodologies**" Kluwer Academic, 1997.

Course Title	**MEMS**				**Course Type**		**Theory**	
Course Code	**M20TLS0234**	**Credits**	**3**		**Class**		**II Semester**	
MEMS	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	**IA**	**SEE**
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

Micro-Electro-Mechanical Systems (MEMS) is a multidisciplinary area that includes a design and fabrication of sensors and actuators which are capable of micron-size mechanical movements. Lectures cover a wide range of topics in design, fabrication and packaging of MEMS.

COURSE OBJECTIVES:

The objectives of this course are:

1. To describe the various MEMS materials, devices and applications.
2. Demonstrate the three fundamental pillars of MEMS, i.e. design, fabrication and micromachining techniques.
3. Evaluate different packaging materials used for MEMS.
4. understand the unique demands, environments and applications of MEMS devices

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	**Course Outcomes**	**POs**	**PSOs**
CO1	Demonstrate the application of scaling laws in the design of microsystems.	1,2,3,4	1,2,3
CO2	Relate to the scaling laws in miniaturization.	1,2,3,4	1,2,3
CO3	Evaluate among different packaging techniques.	1,2,3,4	1,2,3
CO4	Analyze the critical performance aspects of electromechanical transducers, including sensors and actuators.	1,2,3,4	1,2,3
CO5	Understand the various application areas for MEMS devices	1,2,3,4	1,2,3
CO6	Know the design and fabrication processes involved with MEMS devices.	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓	✓			
CO2	✓	✓	✓			
CO3	✓	✓				
CO4	✓	✓	✓			
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	3								1	2	1
CO2	3	1	3	2								3	2	1
CO3	1	3	2	2								1	3	2
CO4	3	3	1	2								3	2	1
CO5	3	1	3	2								3	3	1
CO6	1	3	2	2								3	2	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
Introduction to MEMS Overview of MEMS and Microsystems: What are MEMS, Why Miniaturization, Why microfabrication, Microsystems versus MEMS, Smart Materials, Structures and Systems, Integrated Microsystems, Typical MEMS and Microsystem Products, The Multidisciplinary nature of Microsystem design and manufacture, Applications of smart Materials and Micro Systems, Applications of Aerospace, Biomedical and Automotive industry. **Materials for MEMS:** Silicon compatible material System-Silicon, Czochralski Crystal Growing, Silicon oxide and Nitride, Thin metal Films, Polymers, Other material and substrates.
UNIT - 2
Microsystems Fabrication Process **Epitaxy**: Introduction, Vapor-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation.
UNIT - 3
Microsystems Design and Packaging Assembly, Packaging, and Testing (APT) of Microsystems, Microsystem Packaging, overview o Mechanical Packaging of Microelectronics, interfaces in Microsystem Packaging, Essential Packaging Technologies,Three Dimensiona Packaging, Assembly of Microsystems, Selection of Packaging Materials.

UNIT - 4

Micro Sensors, Actuators, Systems and Smart Materials

Case studies – silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conduct metric gas sensor, silicon micro-mirror arrays, and piezo-electric based inkjet print head, electrostatic comb-drive and magnetic micro relay, portable clinical analyzer, active noise control in a helicopter cabin.

VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC technology, CMOS IC Technology MOS Memory IC Technology, Bipolar IC Technology, IC Fabrication.

References Books:

1. G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre, "Micro and Smart Systems", Wiley India, 2010.
2. Chang Liu, "Foundation of MEMS" Pearson Education International, 2006.
3. Tai Ran Hsu, "MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering, Wiley, 2008.
4. S. M. Sze, "VLSI Technology", McGraw-Hill, Second Edition.
5. Nadim Maluf, Kirt Williams "An Introduction to Microelectromechanical Systems Engineering" Second addition.

<table>
<tr><td>Course Title</td><td colspan="4">High Speed VLSI Design</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td>Course Code</td><td>M20TLS0235</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
<tr><td rowspan="5">High Speed VLSI Design</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

This course introduces the frequency, time and distance issues in digital VLSI. To begin with,the wire delay modeling, geometry and electrical properties of wires, Electrical models of wiresare discussed. State-of-the-art techniques to optimize the performance and energy consumption of a circuit. One or more of these techniques are used in a design project.

COURSE OBJECTIVES:

The objectives of this course are:

1. Introduce the concept of high speed digital circuits.
2. Understand the power distribution and noise sources in VLSI circuits.
3. Understand the importance of timing analysis in high speed VLSI circuits.
4. Introduce the concept of latch and clock driven logic circuits for high speed VLSI circuits.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Describe the electrical characteristics of R L C components in high speed VLSI circuits	1,2,3	1,2,3
CO2	Identify and analyse the sources of noise in VLSI circuits.	1,2,3	1,2,3
CO3	Describe the Signalling modes for transmission lines in VLSI circuits	1,2,3	1,2,3
CO4	Perform the timing analysis for VLSI Circuits.	1,2,3	1,2,3
CO5	Design the clocked and non-clocked logic circuits and design various latch based digital circuits	1,2,3	1,2,3
CO6	Demonstrate and analyze the performance of VLSI circuits at high frequency	1,2,3	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓			✓		
CO3	✓					
CO4	✓			✓		
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2									1	2	1
CO2	3	3	3									3	2	1
CO3	3	3	2									3	3	2
CO4	3	3	2									3	3	1
CO5	1	2	3									2	1	1
CO6	2	1	3									2	1	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents

Introductionto High Speed Digital Design

Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power.Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

UNIT - 2

Power distribution and Noise

Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference.

Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling ove RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

UNIT - 3

Timing fundamentals timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock distribution, clock skew an methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DL based clock aligners.

UNIT - 4

Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass GateLogic, Static CMOS, DCVS Logic Non-Clocked Pass Gate Families.

Latching Strategies: Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logi Asynchronous Latch Techniques.

REFERENCE BOOK:

1. William S. Dally & John W. Poulton, "**Digital Systems Engineering**", *Cambridge University Press*, 1998.
2. Kerry Bernstein &ET. Al., "**High Speed CMOS Design Styles**", Kluwer, 1999.
3. Howard Johnson & Martin Graham, "**High Speed Digital Design**" A Handbook of Black Magic, *Prentice Hall PTR*, 1993.
4. Masakazu Shoji, "**High Speed Digital Circuits**", *Addison Wesley Publishing Company*, 1996.
5. Jan M, Rabaey, et al, "**Digital Integrated Circuits**", A Design Perspective, *Pearson*, 2003.

Course Title	**ASIC Design and Verification using System Verilog**				**Course Type**		**Theory**	
Course Code	**M20TLS0241**	**Credits**	**3**		**Class**		**II Semester**	
ASIC Design and Verification using System Verilog	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course aims to give an in-depth introduction to the SystemVerilog which is an enhancement to the Verilog hardware description language (HDL). It also discusses the benefits of the new features, and demonstrates how design and verification can be more efficient and effective when using System Verilog constructs.

COURSE OBJECTIVES:

The objectives of this course are:

1. To study the verification methodologies and basic concepts of System Verilog.
2. Study the different kinds of procedural statements of System Verilog.
3. Study the basic concepts of OOPs
4. To understand connecting of design and testbench.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Understand the Verification of a DUT and use different kinds of data types in System Verilog.	1,2,3,4,5	1,2,3
CO2	Analyze and test the System Verilog routines and procedural statements.	1,2,3,4,5	1,2
CO3	Understand and apply the basic concepts of OOPs in System Verilog.	1,2,3,4,5	1,2
CO4	Analyze the usefulness of a driver, monitor, checker, test cases in a verification environment.	1,2,3,4,5	1,2,3
CO5	Apply constrained random tests benches using System Verilog	1,2,3,4,5	1,2,3
CO6	Analyze a verification case and apply System Verilog to verify the design	1,2,3,4,5	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓	✓	✓		
CO3	✓				✓	
CO4	✓	✓	✓	✓		
CO5	✓	✓	✓	✓		
CO6	✓	✓	✓	✓		

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	3	1	2	1							1	2	1
CO2	2	3	3	1	2							3	2	
CO3	2	3	2	2	2							3	3	
CO4	3	3	2	2	1							3	3	2
CO5	1	2	3	1	2							3	3	2

CO6	2	3	3	1	2							3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
Introduction The Verification Process, The Verification Plan, The Verification Methodology, Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench, Building a Layered Testbench, Simulation Environment Phases, Maximum Code Reuse, Testbench Performance. Introduction to data types, Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Expression Width, Net Types.
UNIT - 2
System Verilog Introduction, Procedural Statements, Tasks, Functions, and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.
UNIT - 3
System Verilog Introduction, Think of Nouns, not Verbs, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects, Public vs. Private Straying Off Course, Building a Testbench
UNIT - 4
Testing and Verification Introduction, Separating the Testbench and Design, The Interface Construct, Stimulus Timing, Interfac Driving and Sampling, Connecting It All Together, Top-Level Scope, Program – Module Interactions, SystemVerilog Assertions, Th Four-Port ATM Router. Current Trends in Testing and Verification: Advanced verification methodologies, e.g., UVM and OVM at basic levels. Cadence-IUS Mentor-QuestaSim EDA Development Environment.

REFERENCE BOOK:

1. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Publisher: Springer-Verlag New York, Inc. Secaucus, NJ, USA, 2006
2. Donald Thomas, **"Logic Design and Verification Using SystemVerilog**", CreateSpace Independent Publishing Platform, 2014.
3. Language Reference Manual for SystemVerilog.

Course Title	**Embedded Applications in Power Conversion**				**Course Type**		**Theory**	
Course Code	**M20TLS0242**	**Credits**	**3**		**Class**		**II Semester**	
Embedded	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				

Applications In Power Conversion	-	-	--	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

Power Electronics is an Enabling Technology. Today most of the Electrical Energy is processed through Power Electronic Converters at the user end. Due to Increasing Grid Integration of Renewables now the Power Converters are necessary even at the Generation end. Significant amount of effort goes into the Embedded Systems Design of a Modern Complex Power Converter System and requires expertise in areas different from Power Electronic Circuit Design and Control. In this Course, we will learn how to Design an Embedded System for the Real-Time Monitoring, Control and Protection of a typical Power Electronic Conversion System.

COURSE OBJECTIVES:

The objectives of this course are:

1. Study the design of power converters
2. Design of various power converters using embedded systems
3. Design of UPS and DC motor drives

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Describe the electrical characteristics of various power semiconductor devices	1,2,3	1,2,3
CO2	Understand the working of power converters.	1,2,3	1,2,3
CO3	Apply the concepts of embedded systems to design power converters.	1,2,3	1,2,3
CO4	Explore the various parts of UPS and DC motor drives.	1,2,3	1,2,3
CO5	Illustrate the design of DC motor drives	1,2,3	1,2,3
CO6	Explore the recent developments in power conversion systems	1,2,3	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓			✓		
CO3	✓					
CO4	✓	✓				
CO5	✓	✓				
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	1										1	2	1
CO2	3	3	3										3	2	1
CO3	3	3	2										3	3	2
CO4	1	2	3										1	2	2
CO5	2	1	3										3	2	1
CO6	3	1	2										3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT – 1
Power Converters
Power Converters: Power converter system design. Isolated and Non-isolated dc-dc converters. Inverters with square and sinusoidal output. PWM switching – unipolar and bipolar, sine PWM Practical Converter design considerations: Power semiconductor devices – Power Diodes, BJT, MOSFET, IGBT. MOSFET & IGBT – Ratings, SOA, Switching characteristics, Gate Charge, Paralleling devices. Dos and Don'ts of using Power MOSFETs, Gate drive characteristics & requirements of power MOSFETs and IGBT modules. Design of turn on and turn off snubbers. Magnetic components: Design of high frequency transformer, design of Inductors, design of CTs.
UNIT - 2
Design of controllers for Power converters
Design of controllers for Power converters: Micro controllers and DSP based controllers for power conversion. Peripheral interfacing - ADC, Keyboard, LCD display, PWM generation. Design of PWM bridge controller based on low end and high-end controllers. Interfacing of controller output to power module. Designs based on dedicated gate driver ICs. Design of isolated gate drives.
UNIT - 3
Design of UPS
Design of UPS: Online, off line UPS. Operation & design criteria of AC switch, Operation & design criteria of battery charger, operation & design criteria of inverter, active PFC circuits. Thermal design of power converters.
UNIT - 4
DC Motor Drives
DC Motor Drives: Design of adjustable speed DC motor drives, speed control of a separately excited motor, design of closed loop control, design chopper controlled DC motor drive, design of four quadrant chopper. AC Motor Drives: Design of 3 phase PWM VSI inverter, design of v/f control for induction Motor, design of open loop and closed loop control. Vector control of AC motors, space vectors, vector control strategy for induction motor.

REFERENCE BOOK:

1. Power Electronics; By: Mohan, Underland, Robbins; John Wiley & Sons
2. Simplified design of Switching Power supplies; By: John D Lenk; EDN series fordesigners.
3. Design of magnetic components for switched mode power converters; By L Umanad,S.R Bhat; Wiely Eastern ltd.

<table>
<tr><td colspan="2">Course Title</td><td colspan="4">Product Design & Quality Management</td><td colspan="2">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td colspan="2">Course Code</td><td>M20TLS0243</td><td>Credits</td><td colspan="2">3</td><td colspan="2">Class</td><td colspan="2">II Semester</td></tr>
<tr><td rowspan="5">Product Design &Quality Management</td><td>TLP</td><td>Credits</td><td>Contact Hours</td><td>Work Load</td><td colspan="2" rowspan="2">Total Number of Classes Per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Theory</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>Practice</td><td>-</td><td>-</td><td>-</td><td rowspan="2">Theory</td><td rowspan="2">Practical</td><td rowspan="2">IA</td><td rowspan="2">SEE</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Total</td><td>3</td><td>3</td><td>3</td><td>39</td><td>-</td><td>50 %</td><td>50 %</td></tr>
</table>

COURSE OVERVIEW:

Innovation, better management, throughput improvements, and expansion of new technologies have led Product Design and Manufacturing as a compelling field for the students. Managing the product development process, right from idea generation to final product manufacturing has to be systematic and effective to meet the customer needs, while incorporating the time-to-market constraint as well. This course presents an overview of the product design and development process, along with the manufacturing systems aspects. The concepts Design for Manufacturing, Assembly, and Environment, and analytical tools for development, costing and manufacturing would help the students and practitioners learn to conceptualize, design, and manufacture competitively-priced quality products. Reverse Engineering, Prototyping and Simulation using soft tools are also incorporated make the students learn the advanced methods in manufacturing. Finally, the important concept of quality management for products is discussed in detail.

COURSE OBJECTIVES:

The objectives of this course are:

1. Study the Development process, customer needs and product specifications
2. Understand the concept of manufacturing, robus design and IP rights various power converters using embedded systems
3. Analyse the design economy and assuring the quality of the product

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Explore the product design and development life cycle.	1,2,3,7,8	1,2,3
CO2	Understand the robust design. Design economics and paternt/copy right issues.	1,2,3,7,8	1,2,3
CO3	Study various impact of Copy right and patenting on industrial growth	1,2,3,7,8	1,2,3
CO4	Know the continuos process of customer satisfaction and improvement techniques	1,2,3,7,8	1,2,3
CO5	Explore the techniques for statistical processing and benchmarking	1,2,3,7,8	1,2,3

CO6	Describe total quality management in product design	1,2,3,7,8	1,2,3

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓			✓		
CO3	✓				✓	
CO4	✓	✓	✓			
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	1				3	3					1	2	1
CO2	3	3	3				1	2					3	2	1
CO3	3	3	2				2	3					3	3	1
CO4	2	3	1				2	3					2	3	1
CO5	1	2	3				1	2					1	2	3
CO6	2	3	1				2	q					3	1	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT – 1
Product Design and Development: I Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection, Product architecture, Industrial design.
UNIT – 2
Product Design and Development: II Design for Manufacturing, Prototyping, Robust Design, Patents and Intellectual property, Product Development Economics, Managing Product Development Projects.
UNIT – 3
Total Quality Management I Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement. **Tools and Techniques:** Statistical Process Control, Quality Systems, Bench Marking

UNIT – 4

Total Quality Management II

Quality Function Deployment, Product Liability, Failure Mode and Effect Analysis, Management Tools.

REFERENCE BOOK:

1. Total Quality Management, Second edition By: Dale H. Besterfield, PearsonEducation Asia
2. Product Design & Development; Third edition By: Karl T Ulrich & Steven DEppinger; Mc Graw Hill

Course Title	**Embedded Systems In Smart Grid**				**Course Type**		**Theory**	
Course Code	**M20TLS0244**	**Credits**	**3**		**Class**		**II Semester**	
Embedded Systems In Smart Grid	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	**IA**	**SEE**
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

As global energy demand is growing, governments and businesses are increasingly seeking to reduce the world's dependence on fossil fuels. This course helps you to learn electronic engineering in the area of renewable energy systems alongside specialist topics to address these challenges head-on. Students will gain a foundation in theelectronic engineering and core topics like circuit theory and communications systems. The course also allows to build knowledge of areas such as power systems, smart grid systems, and power electronics for renewable systems control and energy conversion.

COURSE OBJECTIVES:

The objectives of this course are:

1. Study the architecture of power systems and its importance
2. Applying the concepts of embedded systems onto smart grids
3. Analysing the role of IoT systems in smart grid

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	**Course Outcomes**	**POs**	**PSOs**
CO1	Understanding the basics of power system management and its automation.	1,2,3	1,2,3
CO2	Explore the features of Smart grid.	1,2,3	1,2,3
CO3	Learn different Sensors and embedded devices used in smart grid.	1,2,3	1,2,3
CO4	Examine the different communication standards, technologies and protocols for smart grid.	1,2,3	1,2,3

CO5	Explore the IoT systems for smart grid systems	1,2,3	1,2,3
CO6	Discuss the new innovative techniques for future smart grid systems	1,2,3	1,2,3

CO#	**Bloom's Level**					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓			✓		
CO3	✓					
CO4	✓			✓		
CO5		✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1									1	2	1
CO2	3	3	3									3	2	1
CO3	3	3	2									3	3	2
CO4	3	3	2									1	3	2
CO5	1	2	2									2	3	1
CO6	1	2	2									3	1	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1
Introduction Smart grid definition.Smart grid vs conventional grid. Smart Grid technologies- Power system and ICT in Generation,Transmission and Distribution. Basic understanding of power systems. Managment aspects (Utility, Operator, Consumer).
UNIT - 2
Evolution of automation in power system Evolution of automation in power system. Smart Grid features- Distributed generation, storage, DD, DR, AMI, WAMS, WACS). Sensors - CT, PT

UNIT - 3
Embedded Devices Embedded Devices - IED, PMU, PDC, CT, PT, relays, DR Switch; Algorithms; Communication- Standards, Technology and protocols. IoT applications in power system – Case study 1 generation control, load management, dynamic pricing etc; IoT for domestic prosumers. Case Study 2 -Smart microgrid simulator (SMGS),DR,DD,Energystorage,Communication.
UNIT - 4
Case Studies And Testbeds For The Smart Grid Introduction, demonstration projects, advanced metering, microgrid with renewable energy, power system unit commitment problem, case study of RER Integration, Testbeds and benchmark systems, chanlleges of smart transmission, benfits of smart transmission

REFERENCE BOOK:

1. James Momoh, “Smart Grid: Fundamentals of Design and Analysis”, Wiley-IEEE Press, March 2012.
2. JanakaEkanayake, Nick Jenkins, KithsiriLiyanage, Jianzhong Wu and Akihiko Yokoyama, “Smart Grid: Technology and Applications”, Wiley, February 2012.
3. NouredineHadjsaïd and Jean-Claude Sabonnadière, “Smart Grids”, Wiley-ISTE, May 2012.
4. Ali Keyhani and Muhammad Marwali, “Smart Power Grids 2011”, Springer, 2011.

Course Title	**Embedded Linux System Design And Development**				**Course Type**		**Theory**	
Course Code	**M20TLS0245**	**Credits**	**3**		**Class**		**II Semester**	
Embedded Linux System Design And Development	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

Linux-based embedded systems are widely used in smartphones, in-vehicle infotainment systems, in countless consumer electronics and for numerous industrial applications. As a result, the demand for qualified embedded system engineers with the requisite experience in Linux is on the rise. This course teaches how to configure the Linux kernel and develop custom peripheral drivers. Learners gain an understanding of the Linux architecture and acquire the practical skills involved in building an embedded Linux system, board supporting packages, embedded storage. The course also focuses to develop the device drivers for various peripherals

COURSE OBJECTIVES:

The objectives of this course are:

1. Understanding the evolution of embeddedLinux.

2. Concepts of GNU cross-platform tool chain
3. Explain the boot loader architecture, system memory map, both hardwareand software memory maps, interrupt management, the PCI subsystem,timers, UART, and power management.
4. Explore the embedded storage
5. Learn the steps to port the applications onto embedded linux

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Knowledge and understanding of Embedded Linux Operating System architecture	1,2,3,4,5	1,2,3
CO2	Ability to choose between different software tools for the development of an embedded	1,2,3,4,5	1,2,3
CO3	Explore the embedded Linux development environment.	1,2,3,4,5	1,2,3
CO4	Create Linux BSP for a hardware platform.	1,2,3,4,5	1,2,3
CO5	Ability to evaluate implementation results (e.g. speed, cost, power) and correlate them with	1,2,3,4,5	1,2,3
CO6	Implement the embedded storage and write drivers and applications targeted to embedded linux.	1,2,3,4,5	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓			✓		
CO3	✓				✓	
CO4	✓	✓				
CO5	✓	✓	✓	✓	✓	
CO6	✓	✓	✓	✓	✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	1	2	1	3							1	2	1
CO2	3	2	1	2	3							3	2	1
CO3	3	3	2	3	1							3	3	1
CO4	1	2	3	1	2							1	2	3
CO5	2	1	3	1	3							3	1	2

CO6	1	3	1	2	1							3	1	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT – 1
Introduction Introduction: History of Embedded Linux, Why Embedded Linux,Embedded Linux Versus Desktop Linux, Embedded Linux Distributions, Porting Roadmap, Architecture of Embedded Linux and KernelArchitecture, User Space, Linux Start-Up Sequence, GNU Cross-Platform Tool chain.
UNIT - 2
Board Support Package (BSP) Board Support Package: Inserting BSP in Kernel BuildProcedure, Memory Map, Interrupt Management, The PCISubsystem, Timers, UART, Power Management
UNIT - 3
Embedded Storage and drivers Embedded Storage: Flash Map, MTD—Memory TechnologyDevice, MTD Architecture, Sample MTD Driver for NOR Flash, TheFlash-Mapping Drivers, MTD Block and Character Devices,Mtdutils Package, Embedded File Systems, Optimizing StorageSpace, Tuning Kernel Memory. **Embedded Drivers:** Linux Serial Driver, Ethernet Driver, I2C and USB on linux, Watchdog Timer, KernelModules.
UNIT - 4
Porting the applications of Linux Porting Applications: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

Course Title	Electronic Packaging				Course Type		Theory	
Course Code	M20TLS0311	Credits	3		Class		III Semester	
Electronic Packaging	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	IA	SEE
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course includes fundamentals of electronic packaging engineering and basic concepts in thermal, mechanical, electrical, and environmental management of modern electronic systems. Emphasis is on high-frequency (and high-speed) package performance and its achievement through the use of advanced analytical tools, proper materials selection, and efficient computer-aided design. Packaging topics include die and lead attachment, substrates, hybrids, surface-mount technology, chip and board environmental protection, connectors, harnesses, and printed and embedded wiring boards. Students develop a fundamental understanding of the basic principles used in the packaging of modern electronics so that when faced with a packaging issue they can recognize the various methods available and perform the tradeoffs necessary to select the appropriate/optimum packaging solution for the application.

COURSE OBJECTIVES:

The objectives of this course are:

1. Understand the concept of electronic packaging and importance of packaging in semiconductor industry
2. Know the various types of packaging and their applications.
3. Analysing the effect of CAD tools on packaging.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Analyze the impact of electronic packaging in semiconductor industry.	1,2,3,4,5,6,7,8	1,2,3
CO2	Explore the different types of packaging for specific requirement.	1,2,3,4,5,6,7,8,9	2,3
CO3	Identifying the different types of failures/faults during packaging.	1,2,6,9	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				

CO2	✓	✓	✓	✓		
CO3	✓				✓	

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	3	1	1	1				1	3	2
CO2	3	3	3	1	1	1	2	2	2				3	2
CO3	3	3				2			1			2	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT - 1 Overview of electronic systems packaging, Definition of a system and history of semiconductors , Products and levels of packaging, Packaging aspects of handheld products; Case studies in applications , Definition of PWB. Video on "Sand-to-Silicon" ,Wafer fabrication, inspection and testing , Wafer packaging; Packaging evolution; Chip connection choices , Wire bonding, TAB and flipchip-1 ,Wire bonding, TAB and flipchip-2.
UNIT - 2 Necessary of packaging. Types , Single chip packages or modules (SCM), Commonly used packages and advanced packages; Materials in packages, Thermal mismatch in packages; Current trends in packaging , Multichip modules (MCM)-types; Systeminpackage (SIP);Packaging roadmaps; Hybrid circuits; Electrical Issues – I; Resistive Parasitic , Electrical Issues – II; Capacitive and Inductive Parasitic , Electrical Issues – III; Layout guidelines and the Reflection problem, Electrical Issues – IV; Interconnection.
UNIT - 3 Benefits from CAD to packages; Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights , Design Flow considerations; Beginning a circuit design with schematic work and component layout , Demo and examples of layout and routing; Technology file generation from CAD; DFM check list and design rules; Design for Reliability. Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates, Substrates continued; Video highlights; Surface preparation, Photoresist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB etching; Resist stripping; Screenprinting technology, Through-hole manufacture process steps; Panel and pattern plating methods.
UNIT - 4 SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave solderin, Vapour phase soldering, BGA soldering and Desoldering/ Repair; SMT failures, SMT failure library and Tin Whiskers, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead-free alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling issues. Thermal Design considerations in systems packaging, Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes Embedded capacitors; Processes for embedding capacitors; Case study.

REFERENCE BOOK:

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY,2001.
2. William D.Brown,Advanced Electronic Packaging, IEEE Press, 1999.

Course Title	Algorithms For VLSI				Course Type		Theory	
Course Code	M20TLS0312	Credits	3		Class		III Semester	
Algorithms For VLSI	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	IA	SEE
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

The course will acquaint the concepts of design flow in VLSI physical design, the basic data structures and algorithms used for implementing the same. The course will also provide examples and assignments related to Graph Algorithm, Computational geometry algorithm, Partitioning and Placements, in order to help the students to understand the concepts involved, and appreciate the main contests therein.

COURSE OBJECTIVES:

The objectives of this course are:

1. To acquaint the basics of various graph principles algorithms.
2. To understand the concepts of data structures, classes, relationship and problems associated with the Computational Geometry algorithms.
3. To articulate the concepts of partitioning, planning and various pin assignments.
4. To illustrate the principles of placements and routing in the chip design process.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Understand the various design methodologies	1,2,3	1,2,3
CO2	Evaluate the computational complexity of an algorithm	1,2,3	1,2,3
CO3	Apply genetic algorithm to various stages of VLSI design such as floor planning, partitioning and placement	1,2,3	1,2,3
CO4	Analyze and compare power estimation using genetic algorithm and comparing its performance with conventional algorithms.	1,2,3	1,2,3
CO5	Validating the various physical design algorithms with respect to placement, partitioning, routing in the IC design.	1,2,3	1,2,3
CO6	Design efficient routing circuits to address the issues in routing congesting, delay and power dissipation.	1,2,3	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓			✓		
CO3	✓					
CO4	✓			✓		
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1									1	2	1
CO2	3	3	3									3	2	1
CO3	3	3	2									3	3	2
CO4	3	3	1									3	3	2
CO5	1	2	3									3	2	1
CO6	3	2	2									3	3	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT - 1 Graph Algorithms: Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm.
UNIT - 2 Computational geometry Algorithms: Line sweep method and extended line sweep method.Basic data structures: Linked list of blocks, Bin based method, neighbor pointers and corner stitching.Graph Algorithms for physical design: Classes of graphs in physical design, relationship between graph classes,graph problems, Algorithms for interval graphs and Algorithms for permutations graphs.
UNIT - 3 Partitioning: Group migration Algorithms.Floor planning and Pin assignment: floor planning, chip planning and pin assignment.

UNIT - 4

Placement: Simulated annealing, simulated evolutions, force directed placement, sequence pair technique,Breuer's Algorithm, Terminal propagation Algorithm, Cluster growth and quadratic assignment.Routing: Maze routing Algorithms: Lee's Algorithm, Soukup's Algorithm and Hadlock's Algorithm. Shortest pathalgorithm, Steiner tree based Algorithm. Single layer routing Algorithms and two layer routing Algorithms.Over the cell routing, Via minimization, clock, power and ground routing.

REFERENCE BOOK:

1. Naveed Sherwani, **"Algorithms for VLSI Physical Design Automation"** 3rd edition, Springer international,1998.
2. Pinaki Mazumber, Elizabeth M Rudnick, "**Genetic Algorithms For VLSI Design, Layout & Test Automation"**,Pearson education,2007

Course Title	**Synthesis and Optimization of Digital Circuits**				**Course Type**		**Theory**	
Course Code	**M20TLS0313**	**Credits**	**3**		**Class**		**III Semester**	
Synthesis and Optimization of Digital Circuits	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

The aim of this course is to present automatic logic synthesis techniques for computer-aided design (CAD) of very large-scale integrated (VLSI) circuits and systems. This course will broadly survey the state of the art, and give a detailed study of various problems, pertaining to the logic-level synthesis of VLSI circuits and systems, including: two-level Boolean network optimization, multi-level Boolean network optimization, technology mapping for library-based designs and field-programmable gate-array (FPGA) designs, and state-assignment and re-timing for sequential circuits. The course will also cover various representations of Boolean functions, such as binary decision diagrams (BDDs), and discuss their applications in logic synthesis

COURSE OBJECTIVES:

The objectives of this course are:

1. To introduce students to basic optimization techniques used in circuits design.
2. To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits
3. To introduce in details Logic-Level synthesis and optimization techniques for combinational and sequential circuits.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	**Course Outcomes**	**POs**	**PSOs**

CO1	Understand the process of synthesis and optimization in a top down approach for digital circuits' models.	1,2,3,4	1,2,3
CO2	Know the terminologies of graph theory and its algorithms to optimize a Boolean equation	1,2,3,4	1,2,3
CO3	Use different two level and multilevel optimization algorithms for combinational circuits	1,2,3,4	1,2,3
CO4	Illustrate the different sequential circuit optimization methods using state models and network models	1,2,3,4	1,2,3
CO5	Demonstrate the scheduling techniques digital circuits	1,2,3,4	1,2,3
CO6	Know the cell library design and binding in design automation	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	**Bloom's Level**					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**
CO1	✓	✓				
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓			
CO4	✓	✓	✓			
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2	2								3	2	3
CO2	3	3	3	1								1	2	3
CO3	3	3	2	1								3	2	3
CO4	3	3	1	3								3	2	3
CO5	2	1	2	3								1	2	3
CO6	1	2	3	1								2	1	3

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT - 1 Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis an optimization. Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems graph optimization problems and algorithms, Boolean algebra and Applications.
UNIT - 2 Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used i synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimizatio techniques. Two Level Combinational Logic Optimization: Logic optimization principles, operation on two level logic covers, algorithms for logic minimization.
UNIT - 3 Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization. Sequential Circuit Optimization: Sequential circuit optimization using state based models, state minimization, and Finite state machine decomposition.
UNIT - 4 A model for scheduling problems, Scheduling without resource constraints, Scheduling algorithms for extended sequencing models Scheduling Pipe lined circuits. Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

REFERENCE BOOK:

1. Giovanni De Micheli, "**Synthesis and Optimization of Digital Circuits**", Tata McGraw-Hill, 2003.
2. ZviKohavi, "**Switching and Finite Automata Theory**", Tata McGraw Hill, thirdedition, 2000.
3. Alan B.Marcovitz, "**Intro. To Logic Design**", TMH, second edition, 2002.
4. Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, "**Logic Synthesis**", McGraw-Hill, USA, 1994.
5. Neil H.E. Weste and David money Harris, "C**MOS VLSI Design: A circuits and system Perspective**", fourth edition, Pearson Education (Asia) Pvt. Ltd., 2000.
6. Kevin Skahill, "**VHDL for Programmable Logic**", Pearson Education (Asia) Pvt. Ltd., 2000.

Course Title	**CMOS RF Circuit Design**				**Course Type**		**Theory**	
Course Code	**M20TLS0314**	**Credits**	**3**		**Class**		**III Semester**	
CMOS RF Circuit Design	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-				
	-	-	-	-	Theory	Practical	**IA**	**SEE**

	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course will introduce the design principles and analysis of CMOS Radio frequency (RF) integrated circuits for communication systems. Students are supposed to understand architectures of RF system and master the keypoint of designing RF circuits will be followed by discussion on transciever architectures (Heterodyne, Direct Conversion, etc.), and review modulation and upconversionconcepts.Besides the system level design considerations for RFIC, this course also present rule-of-thumbs in designing RF main blocks such as Low-Noise-Amplifier (LNA), mixer, Voltage-Controlled-Oscillator (VCO), and Phase-Locked-Loop (PLL).

COURSE OBJECTIVES:

The objectives of this course are:

1. To understanding the various aspects of design and analysis of radio frequency integrated circuits and systems (RFICs) for communication and the trade offs between noise, linearity, and spectral costs.
2. To understand the different modulation techniques, multiple access techniques and transreceiver architectures.
3. To study the behavior of MOSFET devices in RF frequency ranges and model according to their behavior.
4. To present the concepts of design of the basic building blocks of communication module like LNA, Mixers, Oscillators, Power amplifiers, matching and biasing circuits.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Describe and analyze the general challenges in the design of CMOS RF circuits.	1,2,3,4,5	1,2,3
CO2	Compare the various modulation techniques, access techniques and transreceiver architectures and choose appropriate ones for particular applications.	1,2,3,4,5	1,2,3
CO3	Interpret the behavior of passive and active devices to model circuits in RF ranges.	1,2,3,4,5	1,2,3
CO4	Analyze and design the building blocks of RF system like LNA, mixers, VCO, power amplifiers etc	1,2,3	1,2,3
CO5	Explain various receivers and transmitter topologies with their merits and drawbacks.	1,2,3	1,2,3
CO6	Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance	1,2,3	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	**Understand (L2)**	**Apply (L3)**	**Analyze (L4)**	**Evaluate (L5)**	**Create (L6)**

CO1	✓	✓				
CO2	✓		✓	✓		
CO3	✓					
CO4	✓	✓		✓		
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	3	1							1	2	1
CO2	3	3	3	2	3							3	2	1
CO3	3	3	2	3	1							3	3	2
CO4	3	3	1									3	3	2
CO5	1	2	2									1	3	2
CO6	2	3	1									1	2	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT - 1
Introduction to RF Design and Wireless Technology
Design and Applications, Complexity and Choice of Technology**.** Basic concepts in RF design: Nonlinearly and Time Variance Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion**.**
UNIT - 2
RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coheren detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, direc conversion and two-step transmitters.
UNIT - 3
BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations o devices, integrated parasitic elements at high frequencies and their monolithic implementation.

UNIT - 4

RF Circuits Design

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesize architectures

REFERENCE BOOK:

1. B. Razavi, "**RF Microelectronics**" PHI 1998.
2. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
3. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
4. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996.

Course Title	**Advances in VLSI Design**				**Course Type**		**Theory**	
Course Code	**M20TLS0315**	**Credits**	**3**		**Class**		**III Semester**	
Advances in VLSI Design	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	-	-	-	Theory	Practical	**IA**	**SEE**
	-	-	-	-				
	Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

This course provides the overview of advances in VLSI industry. To begin with, it discusses the overview of CMOS circuits and their challenges are discussed. The evolutionary advances beyond CMOS circuits such as carbon nanotubes, tectile computing, quantum computing concepts are discussed. The platform based design concepts alongwith FPGA/ASIC are introduced.

COURSE OBJECTIVES:

The objectives of this course are:

1. To understand the basics and operation of static, comparison between CMOS and BiCMOS.
2. To understand short channel effects.
3. To understand the challenges to CMOS.
4. To understand the super buffers, layouts and technology mapping.

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Learn advanced technologies in the fields of VLSI design with the fundamental concepts.	1,2,3,4	1,2,3
CO2	Apply advanced technical knowledge in multiple contexts.	1,2,3,4	1, 2,3
CO3	Understand and design advanced VLSI based system and analyze and interpret results.	1,2,3,4	1,2,3
CO4	Use the techniques, skills, modern Electronic Design.	1,2,3,4	1,2,3
CO5	Illustrate the techniques to control the switching events to meet the desired timing constraints using synchronous, clocked approach.	1,2,3,4	1,2,3
CO6	Describe the role of decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories.	1,2,3,4	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓			
CO4	✓	✓		✓		
CO5	✓	✓	✓			
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2								3	2	3
CO2	3	3	3	1								1	2	3
CO3	3	3	1	2								3	2	3
CO4	3	1	1	3								3	2	3

CO5	1	2	3	1								1	2	1
CO6	2	1	3	1								2	3	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents
UNIT – 1
Review of MOS CircuitsMOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS. Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS Miniaturization.
UNIT - 2
Beyond CMOS Evolutionary advances beyond CMOS, carbon Nanotubes, conventional vs. tactile computing, computing, molecula and biological computing - molecular Diode and diode- diode logic. Defect tolerant computing. Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks -NMOS and CMOS functional blocks.
UNIT - 3
Special Circuit Layouts and Technology Mapping Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMO Multiplexers, Barrel shifter, Wire routing and module layout.
UNIT - 4
System DesignCMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate array standard cell approach, Full custom design.

REFERENCE BOOK:

Kevin F Brennan "**Introduction to Semi-Conductor Device**", Cambridge publications, 2006.
2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications, 1990.
3. D.APucknell. "**Basic VLSI Design**", PHI Publication, 2005.
4. Wayne Wolf, "**Modern VLSI Design**" Pearson Education, Second Edition, 2002.

Course Title	**Automotive Electronics System**				**Course Type**	**Theory**
Course Code	**M20TLO0301**	**Credits**	**3**		**Class**	**III Semester**
Automotive Electronics System	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester	Assessment in Weightage
	Theory	3	3	3		

Practice	-	-	-				
-	-	-	-	Theory	Practical	**IA**	**SEE**
Total	**3**	**3**	**3**	**39**	**-**	**50 %**	**50 %**

COURSE OVERVIEW:

The Basic Electrical and Electronics typically deals with the study of Electrical parameters like AC and DC voltage and current and behaviour of voltage and current in passive elements also in active elements like: BJT, Diodes and FET. The concepts of Electromotive force and Magnetomotive force generated in motors, generators and transformers are explained. The concepts of electrical circuits and electromagnetism are applied to analyze the complex problems arise in the power system networks. Through this course Students will get extensive exposure to digital and analog electronics basics.

COURSE OBJECTIVES:

The objectives of this course are:

1. Understand the functions of electronic systems in modern automobiles, modern electronics technology to improve the performance, safety, comfort and related issues
2. Study the principles of automotive sensors and interfacing techniques, design, model and simulate interfacing systems with sensors
3. Know the principles and functionalities of various Automotive Communication Protocols (ACPs), Design ACP based In-Vehicle Networks(IVNs), selection of ACPs for various application in Automotive
4. Know the industry standard practices for ECU design for automotive, modeling and analysis of application software for ECU design and development, design of ECUs for automobiles, design of HIL and fault diagnostics

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Summarize an overview of automotive components, subsystems, design cycles and basics of Electronic Engine Control in today's automotive industry.	1,2,3	1,2,3
CO2	Illustrate sensors, actuators and control systems used in automobiles	1,2,3	1,2,3
CO3	Discuss the role of electronics in engine control systems	1,2,3	1,2,3
CO4	Implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts and get fair idea on future Automotive Electronic Systems.	1,2,3	1,2,3
CO5	Describe the principles and functionalities of communication protocols	1,2,3	1,2,3
CO6	Study the industry standard practices for Electronic Control Unit	1,2,3	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

	Bloom's Level

CO#	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓				
CO2	✓	✓	✓	✓		
CO3	✓					
CO4	✓	✓	✓	✓		
CO5	✓	✓				
CO6	✓	✓				

COURSE ARTICULATION MATRIX

CO#/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1									1	2	1
CO2	3	3	3									3	2	1
CO3	3	3	2									3	3	2
CO4	3	3	1									3	3	1
CO5	2	1	1									2	1	3
CO6	2	1	3									3	1	2

Note:1-Low,2-Medium,3-High

COURSE CONTENT

THEORY:

Contents
UNIT – 1
Automotive Industry and Modern Automotive Systems Vehicle classifications and specifications, need for electronics in automobiles, Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Spark and Compression Ignition Engines, Ignition systems, Spark plug, Spark pulse generation, Ignition Timing. Transmission Control - Automotive transmissions, Drive Train, Brakes, Steering System - Steering Control, Starting System- Battery, Air/Fuel Systems, Fuel Handling, Air Intake System, Lighting.
UNIT – 2
Introduction to Automotive Sensors and Instrumentation Sensors and actuators, Air/ Fuel Management Sensors – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor Sensors in Engine control, adaptive cruise control, braking control, traction control, steering, stability, Lighting, wipers, climate control, Sensors for occupant safety, Sensor and actuator interfacing techniques and electronic displays. Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

UNIT - 3

Control Systems

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control Communication – Serial Data, Communication Systems, Power windows, Remote keyless entry systems, GPS,Automotive Communication Protocols Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, Vehicle Motion Control – Cruise Control, Chassis, , Power Brakes, antilock braking systems, Electronic stability and other technologies, Traction Control, Electronic Stability Control, Electronically controlled suspension Fundamentals of electronically controlled steering system, Power Steering,

UNIT - 4

Safety and Convenience

Electronics for Passenger Safety and Convenience – SIR, Air bag and seat belt pretension systems, Tire pressure monitoring systems, Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters Integrated Body – Climate Control Systems, Electronic HVAC Systems, Lighting, Entertainment Systems Automotive Diagnostics – Timing Light, Engine Analyzer, Process of Automotive Fault Diagnostics, Fault Codes, On-board diagnostics, Off-board diagnostics, Expert Systems. Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System, AFS.

REFERENCE BOOK:

1. Denton. Burlington "**Automotive Electrical and Electronic Systems**", MA 01803, Elsevier Butterworth-Heinemann, 2004.
2. Ronald K. Jurgen. "**Automotive Electronics Handbook**", 2nd Edition, McGraw-Hill, 2007
3. Christian Kohler, "**Enhancing Embedded Systems Simulation**" Vieweg+TeubnerVerlag/ Springer, 2011.
4. Gabriela Nicolescu and Pieter J. Mosterman, "**Model-Based Design for Embedded Systems**", CRC Press, 2010
5. Gilbert Held, "**Inter- and Intra-Vehicle Communications**", CRC Press, 2007.
6. William B. Ribbens, "**Understanding Automotive Electronics**", 5th Edition, Newnes, 2006
7. Bosch, "**Automotive Electrics & Electronics**", Robert Bosch GmbH, 3rd Edition, 1999.

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