REVA UNIVERSITY
Bengaluru, India

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

M. TECH IN VLSI & EMBEDDED SYSTEMS-PT

HAND BOOK: 2019-22

Rukmini Educational
Charitable Trust

Rukmini Knowledge Park
Kattigenahalli, Yelahanka,
Bengaluru – 560064, INDIA

Tel : +91 80 6622 6622
Fax : +91 80 4696 6998

www.reva.edu.in

OUR VISION

REVA University aspires to become an innovative university by developing excellent human resources with leadership qualities, ethical and moral values, research culture and innovative skills through higher education of global standards.

OUR MISSION

1. To create excellent infrastructure facilities and state- of- the -art laboratories and incubation centers .
2. To provide student-centric learning environment through innovative pedagogy and educational reforms.
3. To encourage research and entrepreneurship through collaborations and extension activities.
4. To promote industry-institute partnerships and share knowledge for innovation and development.
5. To organize social development programs for knowledge enhancement in thrust areas.
6. To enhance leadership qualities among youth, to enrich personality traits and promote patriotism and moral values;

BROAD OBJECTIVES

1. Creation, preservation and dissemination of knowledge and attainment of excellence in different disciplines.
2. Smooth transition from teacher - centric focus to learner - centric processes and activities.
3. Performing all the functions of interest to its major constituents like faculty, staff, students and society to reach leadership positions.
4. Developing a sense of ethics in the University community, making it conscious of its obligations to society and the nation.
5. Accepting the challenges of globalization to offer high quality education and other services in a competitive manner.

DO'S AND DON'TS

DO'S

1. Maintain discipline and respect the rules and regulations of the university
2. Be regular and punctual to classes
3. Study regularly and submit assignments on time
4. Be respectful to your Teaches/friends and hostel staff/management.
5. Read the notice board (both at your college and the hostel) regularly.
6. Utilize your Personal Computer for educational purpose only.
7. Follow the code of conduct.
8. Visit Health Center on the campus whenever you are unwell.
9. Be security conscious and take care of your valuables especially Cash, Mobile Phones, Laptop andother valuables.
10. Carry your valuables along with you whenever you proceed on leave/vacation.
11. Use electric appliances, lights and water optimally.
12. Keep the campus clean and hygienic.
13. Use decent dressing.

DON'TS

1. Ragging inside / outside the campus.
2. Possession of Fire arms and daggers etc.
3. Use of Alcohols, Toxic drugs, sheesha, gutkha and hashish/heroin etc.
4. Use of Crackers, explosives and ammUNIT - ion etc.
5. Smoking and keeping any kind of such items.
6. Misusing college & hostel premises/facilities for activities other than studies.
7. Playing loud music in the room which may disturb studies of colleagues / neighbours.
8. Making noise and raising slogans.
9. Keeping electrical appliances, other than authorized ones.
10. Involvement in politics, ethnic, sectarian and other undesirable activities.
11. Proxy in any manner.
12. Use of mobiles in the academic areas.

Note: 1. Rules are revised / reviewed as and when required.
2. Healthy suggestions are welcome for betterment of Institution

REVA UNIVERSITY
Bengaluru, India

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech. (VLSI & Embedded Systems)

Part Time)

HANDBOOK

2019-2022

Rukmini Knowledge Park,
Kattigenahalli, Yelahanka, Bangalore - 560 064
Phone No: +91-080-66226622, Fax: 080-28478539

CONTENTS

Chancellor's Message

"Education is the most powerful weapon which you can use to change the world."

- Nelson Mandela.

There was a time when survival depended on just the realization of physiological needs. We are indeed privileged to exist in a time when 'intellectual gratification' has become indispensable. Information is easily attainable for the soul that is curious enough to go look for it. Technological boons enable information availability anywhere anytime. The difference, however, lies between those who look for information and those who look for knowledge.

It is deemed virtuous to serve seekers of knowledge and as educators it is in the ethos at REVA University to empower every learner who chooses to enter our portals. Driven by our founding philosophy of 'Knowledge is Power', we believe in building a community of perpetual learners by enabling them to look beyond their abilities and achieve what they assumed impossible.

India has always been beheld as a brewing pot of unbelievable talent, acute intellect and immense potential. All it takes to turn those qualities into power is a spark of opportunity. Being at a University is an exciting and rewarding experience with opportunities to nurture abilities, challenge cognizance and gain competence.

For any University, the structure of excellence lies in the transitional abilities of its faculty and its facility. I'm always in awe of the efforts that our academic board puts in to develop the team of subject matter experts at REVA. My faculty colleagues understand our core vision of empowering our future generation to be ethically, morally and intellectually elite. They practice the art of teaching with a student-centered and transformational approach. The excellent infrastructure at the University, both educational and extra-curricular, magnificently demonstrates the importance of ambience in facilitating focused learning for our students.

A famous British politician and author from the 19th century - Benjamin Disraeli, once said 'A University should be a place of light, of liberty and of learning'. Centuries later this dictum still inspires me and I believe, it takes team-work to build successful institutions. I welcome you to REVA University to join hands in laying the foundation of your future with values, wisdom and knowledge.

Dr. P. Shyama Raju
Founder and Hon'ble Chancellor, REVA University

Vice-Chancellor's Message

The last two decades have seen a remarkable growth in higher education in India and across the globe. The move towards inter- disciplinary studies and interactive learning have opened up several options as well as created multiple challenges. India is at a juncture where a huge population of young crowd is opting for higher education. With the tremendous growth of privatization of education in India, the major focus is on creating a platform for quality in knowledge enhancement and bridging the gap between academia and industry.

A strong believer and practitioner of the dictum "Knowledge is Power", REVA University has been on the path of delivering quality education by developing the young human resources on the foundation of ethical and moral values, while boosting their leadership qualities, research culture and innovative skills. Built on a sprawling 45 acres of green campus, this 'temple of learning' has excellent and state-of-the-art infrastructure facilities conducive to higher teaching-learning environment and research. The main objective of the University is to provide higher education of global standards and hence, all the programs are designed to meet international standards. Highly experienced and qualified faculty members, continuously engaged in the maintenance and enhancement of student-centric learning environment through innovative pedagogy, form the backbone of the University.

All the programs offered by REVA University follow the Choice Based Credit System (CBCS) with Outcome Based Approach. The flexibility in the curriculum has been designed with industry-specific goals in mind and the educator enjoys complete freedom to appropriate the syllabus by incorporating the latest knowledge and stimulating the creative minds of the students. Bench marked with the course of studies of various institutions of repute, our curriculum is extremely contemporary and is a culmination of efforts of great think-tanks - a large number of faculty members, experts from industries and research level organizations. The evaluation mechanism employs continuous assessment with grade point averages. We believe sincerely that it will meet the aspirations of all stakeholders – students, parents and the employers of the graduates and postgraduates of Reva University.

At REVA University, research, consultancy and innovation are regarded as our pillars of success. Most of the faculty members of the University are involved in research by attracting funded projects from various research level organizations like DST, VGST, DBT, DRDO, AICTE and industries. The outcome of the

research is passed on to students through live projects from industries. The entrepreneurial zeal of the students is encouraged and nurtured through EDPs and EACs.

REVA University has entered into collaboration with many prominent industries to bridge the gap between industry and University. Regular visits to industries and mandatory internship with industries have helped our students. REVA University has entered into collaboration with many prominent industries to bridge the gap between industry and University. Regular visits to industries and mandatory internship with industries have helped our students become skilled with relevant to industry requirements. Structured training programs on soft-skills and preparatory training for competitive exams are offered here to make students more employable. 100% placement of eligible students speaks the effectiveness of these programs. The entrepreneurship development activities and establishment of "Technology Incubation Centers" in the University extend full support to the budding entrepreneurs to nurture their ideas and establish an enterprise.

With firm faith in the saying, "Intelligence plus character –that is the goal of education" (Martin Luther King, Jr.), I strongly believe REVA University is marching ahead in the right direction, providing a holistic education to the future generation and playing a positive role in nation building. We reiterate our endeavor to provide premium quality education accessible to all and an environment for the growth of over-all personality development leading to generating "GLOBAL PROFESSIONALS".

Welcome to the portals of REVA University!

Director's –Message

Since the inception of REVA University, School of Electronics and Communication Engineering is involved in implementing following best practices in various dimensions such asacademics, research, outreach activities, student development programs, project based and research based learning, student centric learning, student competitions, industry and in-house internships, abroad internships, skill enhancement activities, motivation for competitive exams, mini projects, major projects, industry mentored projects, multidisciplinary projects, industry visits, technical talks by industry and academicians, certification programs, etc.Individual students are taken care by strong mentoring system wherein faculty members are not only allotted as mentorsto students, but also they will act as local guardians and they will have constant follow up with mentees in regard to academic and personal issues till students complete the degree.

The curriculum is carefully designed to meet the current industry trends and also to provide insight into future technology developments that lead to inculcate lifelong learning abilities in students. Board of Studies (BoS) comprises people from academics, industry, alumni and current students which form the strong backbone for our programs wherein constant updates happen in contents/subjects every semester based on current industry needs. Curriculum has good mix of foundation courses, hardcore courses, softcore courses, practicals and projects along with open electives, softskill and skill development courses.

Student's welfare is given utmost priority at School of Electronics and Communication Engineering. Advanced learning methods are adopted to make learning truly interactive. More focus is on discussion and practical applications rather than rote learning. Notes/handouts/video contents/quizzes are given and critical thinking questions are asked to test understanding. Experienced, well qualified and friendly faculty members always strive hard to provide best of education to students. The faculty members have number of publications in reputed national and international journals/conferences. The school is also involved in funded research projects. I am sure the students choosing B Tech and M. Tech programs in School of Electronics and Communication Engineering in REVA University will enjoy the curriculum, teaching and learning environment, well equipped laboratories, digital classrooms infrastructure and the experienced teachers involvement and guidance.

The curriculum caters to and has relevance to local, regional, national, global, developmental need. Maximum number of courses are integrated with cross cutting issues with relevant to professional Ethics, Gender, Human values, Environment, and Sustainability.

Dr. Rajashekhar C. Biradar
Director
School of Electronics and Communication Engineering

PREFACE

The M. Tech in VLSI and Embedded System is designed keeping in view the current situation and possible future developments, both at national and international levels. This course is designed to give greater emphasis on VLSI and Embedded System design with a flexibility to explore any of the implementation platform and application field through a number of soft core courses providing knowledge in these specialized areas. This facilitates the students to choose specialized areas of their interest. Adequate attention is given to provide students the basic concepts and requisite skills.

The area of VLSI design has gained enormous popularity over the past few decades due to the rapid advancements in integrated circuit (IC) design and technology. The ability to produce miniaturized circuits with high performance in terms of power and speed is the reason for its popularity. Using ASIC technology, it has been possible to develop high performance multi-core processors. Verification and testing of such complex designs is a critical and challenging task to ensure the quality of the resulting circuits. The advances in EDA software and CAD tools alleviate the effort necessary to carry out the cumbersome design and verification process of ICs.

The program is designed to expose students to various courses having applications in VLSI and Embedded System like Digital VLSI design, ASIC design, SOC design, Low Power VLSI, High Speed VLSI design, VLSI Testing and verification, CMOS RF Circuit design, Low Power Embedded system. They are also exposed to basic concepts of NANO technology, VLSI testing and Verification, fabrication process ,MEMS, Application specific design and embedded platform like ARM, MSP430, low power microcontrollers and FPGA, through outcome based teaching and learning process which emphasizes practical exposure rather than memorization. A variety of activities such as mini projects, seminars, internships, certification programs, etc. in consultation with industries will be carried out. There is also a scope for cultural, social and community service activities for the students to shape their personality suitable for all-round development.

The VLSI and Embedded System students can choose their career in any VLSI and Embedded System development industries. Now a days almost every appliance is coming with some VLSI component. The scope of VLSI and Embedded System is very wide covering almost every home appliances, industry, automotives, and medical appliance manufactures industry automation and control, telecommunication, **Computer and Digital Systems**, defense and space exploration.

I am sure the students choosing M Tech in VLSI and Embedded System in School of Electronics and Communication Engineering in REVA University will enjoy the curriculum, teaching and learning environment, the vast infrastructure and the experienced teachers involvement and guidance. We will strive to provide all needed comfort and congenial environment for their studies. I wish all students pleasant stay in REVA and grand success in their career.

RUKMINI EDUCATIONAL CHARITABLE TRUST

It was the dream of late Smt. RukminiShyamaRaju to impart education to millions of underprivileged children as she knew the importance of education in the contemporary society. The dream of Smt. RukminiShyamaRaju came true with the establishment of Rukmini Educational Charitable Trust (RECT), in the year 2002. **Rukmini Educational Charitable Trust** (RECT) is a Public Charitable Trust, set up in 2002 with the objective of promoting, establishing and conducting academic activities in the fields of Arts, Architecture, Commerce, Education, Engineering, Environmental Science, Legal Studies, Management and Science & Technology, among others. In furtherance of these objectives, the Trust has set up the REVA Group of Educational Institutions comprising of REVA Institute of Technology & Management (RITM), REVA Institute of Science and Management (RISM), REVA Institute of Management Studies (RIMS), REVA Institute of Education (RIE), REVA First Grade College (RFGC), REVA Independent PU College at Kattigenahalli, Ganganagar and Sanjaynagar and now REVA University. Through these institutions, the Trust seeks to fulfill its vision of providing world class education and create abundant opportunities for the youth of this nation to excel in the areas of Arts, Architecture, Commerce, Education, Engineering, Environmental Science, Legal Studies, Management and Science & Technology.

Every great human enterprise is powered by the vision of one or more extraordinary individuals and is sustained by the people who derive their motivation from the founders. The Chairman of the Trust is Dr. P. ShyamaRaju, a developer and builder of repute, a captain of the industry in his own right and the Chairman and Managing Director of the DivyaSree Group of companies. The idea of creating these top notched educational institutions was born of the philanthropic instincts of Dr. P. ShyamaRaju to do public good, quite in keeping with his support to other socially relevant charities such as maintaining the Richmond road park, building and donating a police station, gifting assets to organizations providing accident and trauma care, to name a few.

The Rukmini Educational Charitable Trust drives with the main aim to help students who are in pursuit of quality education for life. REVA is today a family of ten institutions providing education from PU to Post Graduation and Research leading to PhD degrees. REVA has well qualified experienced teaching faculty of whom majority are doctorates. The faculty is supported by committed administrative and technical staff. Over 13,000 students study various courses across REVA's three campuses equipped with exemplary state-of-the-art infrastructure and conducive environment for the knowledge driven community.

ABOUT REVA UNIVERSITY

REVA University has been established under the REVA University Act, 2012 of Government of Karnataka and notified in Karnataka State Gazette No. 80 dated 27thFebruary, 2013. The University is empowered by UGC to award degrees any branch of knowledge under Sec.22 of the UGC Act. The University is a Member of Association of Indian Universities, New Delhi. The main objective of the University is to prepare students with knowledge, wisdom and patriotism to face the global challenges and become the top leaders of the country and the globe in different fields.

REVA University located in between Kempegowda International Airport and Bangalore city, has a sprawling green campus spread over 45 acres of land and equipped with state-of-the-art infrastructure that provide conducive environment for higher learning and research. The REVA campus has well equipped laboratories, custom-built teaching facilities, fully air-conditioned library and central computer centre, the well planned sports facility with cricket ground, running track & variety of indoor and outdoor sports activities, facilities for cultural programs. The unique feature of REVA campus is the largest residential facility for students, faculty members and supportive staff.

The University is presently offering 23 Post Graduate Degree programs, 20 Degree and PG Degree programs in various branches of studies and has 14000+ students studying in various branches of knowledge at graduate and post graduate level and 400 Scholars pursuing research leading to PhD in 21 disciplines. It has 900+ well qualified, experienced and committed faculty members of whom majority are doctorates in their respective areas and most of them are guiding students pursuing research leading to PhD.

The programs being offered by the REVA University are well planned and designed after detailed study with emphasis with knowledge assimilation, applications, global job market and their social relevance. Highly qualified, experienced faculty and scholars from reputed universities / institutions, experts from industries and business sectors have contributed in preparing the scheme of instruction and detailed curricula for this program. Greater emphasis on practice in respective areas and skill development to suit to respective job environment has been given while designing the curricula. The Choice Based Credit System and Continuous Assessment Graded Pattern (CBCS – CAGP) of education has been introduced in all programs to facilitate students to opt for subjects of their choice in addition to the core subjects of the study and prepare them with

needed skills. The system also allows students to move forward under the fast track for those who have the capabilities to surpass others. These programs are taught by well experienced qualified faculty supported by the experts from industries, business sectors and such other organizations. REVA University has also initiated many supportive measures such as bridge courses, special coaching, remedial classes, etc., for slow learners so as to give them the needed input and build in them confidence and courage to move forward and accomplish success in their career. The University has also entered into MOUs with many industries, business firms and other institutions seeking their help in imparting quality education through practice, internship and also assisting students' placements.

REVA University recognizing the fact that research, development and innovation are the important functions of any university has established an independent Research and Innovation division headed by a senior professor as Dean of Research and Innovation. This division facilitates all faculty members and research scholars to undertake innovative research projects in engineering, science & technology and other areas of study. The interdisciplinary-multidisciplinary research is given the top most priority. The division continuously liaisons between various funding agencies, R&D Institutions, Industries and faculty members of REVA University to facilitate undertaking innovative projects. It encourages student research projects by forming different research groups under the guidance of senior faculty members. Some of the core areas of research wherein our young faculty members are working include Data Mining, Cloud Computing, Image Processing, Network Security, VLSI and Embedded Systems, Wireless Censor Networks, Computer Networks, IOT, MEMS, Nano- Electronics, Wireless Communications, Bio-fuels, Nano-technology for coatings, Composites, Vibration Energies, Electric Vehicles, Multilevel Inverter Application, Battery Management System, LED Lightings, Renewable Energy Sources and Active Filter, Innovative Concrete Reinforcement, Electro Chemical Synthesis, Energy Conversion Devices, Nano-structural Materials, Photo-electrochemical Hydrogen generation, Pesticide Residue Analysis, Nano materials, Photonics, Nana Tribology, Fuel Mechanics, Operation Research, Graph theory, Strategic Leadership and Innovative Entrepreneurship, Functional Development Management, Resource Management and Sustainable Development, Cyber Security, General Studies, Feminism, Computer Assisted Language Teaching, Culture Studies etc.

The REVA University has also given utmost importance to develop the much required skills through variety of training programs, industrial practice, case studies and such other activities that induce the said skills among all students. A full-fledged Career Development and Placement (CDC) department with world class infrastructure, headed by a dynamic experienced Professor & Dean, and supported by well experienced Trainers, Counselors and Placement Officers.

The University also has University-Industry Interaction and Skill Development Centre headed by a Senior Professor & Director facilitating skill related training to REVA students and other unemployed students. The University has been recognised as a Centre of Skill Development and Training by NSDC (National Skill Development Corporation) under PradhanMantriKaushalVikasYojana. The Centre conducts several add-on courses in challenging areas of development. It is always active in facilitating student's variety of Skill Development Training programs.

The University has collaborations with Industries, universities abroad, research institutions, corporate training organizations, and Government agencies such as Florida International University, Okalahoma State University, Western Connecticut University, University of Alabama, Huntsville, Oracle India Ltd, Texas Instruments, Nokia University Relations, EMC^2, VMware, SAP, Apollo etc, to facilitate student exchange and teacher–scholar exchange programs and conduct training programs. These collaborations with foreign universities also facilitates students to study some of the programs partly in REVA University and partly in foreign university, viz, M.S in Computer Science one year in REVA University and the next year in the University of Alabama, Huntsville, USA.

The University has also given greater importance to quality in education, research, administration and all activities of the university. Therefore, it has established an independent Internal Quality division
headed by a senior professor as Dean of Internal Quality. The division works on planning, designing and developing different quality tools, implementing them and monitoring the implementation of these quality tools. It concentrates on training entire faculty to adopt the new tools and implement their use. The division further works on introducing various examination and administrative reforms.

To motivate the youth and transform them to become innovative entrepreneurs, successful leaders of tomorrow and committed citizens of the country, REVA organizes interaction between students and successful industrialists, entrepreneurs, scientists and such others from time to time. As a part of this exercise great personalities such as Bharat Ratna Prof. C. N. R. Rao, a renowned Scientist, Dr. N R Narayana Murthy, Founder and Chairman and Mentor of Infosys, Dr. K Kasturirangan, Former Chairman ISRO, Member of Planning Commission, Government of India, Dr. Balaram, Former Director IISc., and noted Scientist, Dr. V S Ramamurthy, Former Secretary, DST, Government of India, Dr. V K Aatre, noted Scientist and former head of the DRDO and Scientific Advisor to the Ministry of Defence Dr. Sathish Reddy, Scientific Advisor, Ministry of Defence, New Delhi and many others have accepted our invitation and blessed our students and faculty members by their inspiring addresses and interaction.

As a part of our effort in motivating and inspiring youth of today, REVA University also has instituted awards and prizes to recognize the services of teachers, researchers, scientists, entrepreneurs, social workers and such others who have contributed richly for the development of the society and progress of the country. One of such award instituted by REVA University is **'Life Time Achievement Award'** to be awarded to successful personalities who have made mark in their field of work. This award is presented on occasion of the **"Founders' Day Celebration"** of REVA University on 6th January of every year in presence of dignitaries, faculty members and students gathering. The first "REVA Life Time Achievement Award" for the year 2015 has been awarded to Shri. Kiran Kumar, Chairman ISRO, followed by Shri. Shekhar Gupta, renowned Journalist for the year 2016, Dr K J Yesudas, renowned play back singer for the year 2017. REVA also introduced "**REVA Award of Excellence"** in the year 2017 and the first Awardee of this prestigious award is ShriRamesh Aravind, Actor, Producer, Director, Screen Writer and Speaker.

REVA organises various cultural programs to promote culture, tradition, ethical and moral values to our students. During such cultural events the students are given opportunities to unfold their hidden talents and motivate them to contribute innovative ideas for the progress of the society. One of such cultural events is REVOTSAVA conducted every year. The event not only gives opportunities to students of REVA but also students of other Universities and Colleges. During three days of this mega event students participate in debates, Quizzes, Group discussion, Seminars, exhibitions and variety of cultural events. Another important event is ShubhaVidaaya, - Graduation Day for the final year students of all the programs, wherein, the outgoing students are felicitated and are addressed by eminent personalities to take their future career in a right spirit, to be the good citizens and dedicate themselves to serve the society and make a mark in their respective spheres of activities. During this occasion, the students who have achieved top ranks and won medals and prizes in academic, cultural and sports activities are also recognised by distributing awards and prizes. The founders have also instituted medals and prizes for sports achievers every year. The physical education department conducts regular yoga classes everyday to students, faculty members, administrative staff and their family members and organizes yoga camps for villagers around.

Recognizing the fast growth of the university and its quality in imparting higher education, the BERG (Business Excellence and Research Group), Singapore has awarded BERG Education Award 2015 to REVA University under Private Universities category. The University has also been honoured with many more such honors and recognitions.

ABOUT SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

The School of Electronics and Communication Engineering headed by a highly experienced Professor and is supported by well qualified faculty members. The school has the state-of-art class rooms and well equipped laboratories. It offers B.Tech and M.Tech and PhD programs in various specialized streams. The curriculum of both graduate and post graduate degree programs have been designed to bridge the gap between industry – academia and hence they are industry application oriented. The B. Tech program aims to prepare human resources to play a leading role in the continuing adventure of modern automated systems and communications. The Master degree programs focus on research and design in the core and IT industries, building and marketing the next generation of product development. This is reflected in various core subjects offered within the program. B. Tech program offers numerous choices of study for the students based on interest in the current state of art technology. Apart from fundamental courses in Electronics and Communication Engineering, the school facilitates to study in four streams such as Circuits and Devices, Communication Engineering, Signal Processing and Programming. Students are at liberty to choose from these streams in higher semesters. However, there is no restriction of cross migration from one stream to another at any level and thus there is a flexibility provided in the course duration.

The faculty members have number of publications in reputed national and international journals/conferences. The school is also involved in funded research projects. The other important features of the school are individual counseling of students for academic performance, additional coaching classes for important subjects for all the semesters, soft skill development classes, scientific and student centered teaching-learning process.

Student's welfare is given utmost priority at School of Electronics and Communication Engineering. Advanced learning methods are adopted to make learning truly interactive. More focus is on discussion and practical applications rather than rote learning. Notes/handouts are given and critical thinking questions are asked to test understanding. Experienced, well qualified and friendly faculty members always strive hard to provide best of education to students.

Vision

The School of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering blended by research and innovation in tune with changing technological and cultural challenges supported with leadership qualities, ethical and moral values.

Mission

- Establish a unique learning environment to enable the students to face the challenges of the Electronics and Communication Engineering field.
- Promote the establishment of centers of excellence in niche technology areas to nurture the spirit of innovation and creativity among faculty and students.
- Provide ethical and value based education by promoting activities addressing the societal needs.
- Enable students to develop skills to solve complex technological problems of current times and also provide a framework for promoting collaborative and multidisciplinary activities.

ADVISORY BOARD

Sl. No	Name and Affiliation
1	Dr. M.H.Kori, Technology Consultant, Technology Adviser Validus Technologies USA, Retd. Technical Director, Alcatel-Lucent Technologies, Bengaluru
2	Mr. VinodChippalakatti, Vice President, CENTUM Electronics, Bengaluru
3	Dr. MadhusudhnaRao, Group Director & Chief Coordinator (LCA AF), ADA, Bengaluru
4	Dr. ShirshuVarma Professor, Department of Computer Science and Engineering IIIT Allahabad
5	Dr. Rathna G. N. Principal Research Scientist, Department of Electrical Engineering IISc., Bengaluru
6	Mr. Goutham Kumar , Head of Electronics,RLE India
7	Dr. Girish Kumar, Professor, Electrical Engineering, IIT Bombay
8	Dr. MuralidharaKulkarni Department of Electronics & Communication Engineering, NITK, Surathkal
9	Dr. G. S. Javed, Terminus Circuits, Bengaluru
10	Dr. Shivashankar, SECE, VIT Vellore
11	Mr.Aravinda Sharma, Manager,Delphi Systems, Bengaluru
12	Dr. Kashinath, Director, ALS Semiconductors, Bengaluru
13	Mr.LokeshaRai K, Director, Symphony Telecca Services, Bengaluru
14	SanjeevKubakaddi, Itie Solutions, Bengaluru

Programme Overview

Electronics and Communication Engineering is an engineering discipline involved design, development, manufacture and deployment of Electronic and Communication systems. It deals with electronic devices, circuits, communication equipment like transmitter, receiver, integrated circuits (IC), analog and digital transmission and reception of data, voice and video, microprocessors, satellite communication, microwave engineering, antennae and wave progression. Signal and Image processing, Communication Technologies, Embedded Systems, VLSI Systems are some of the specialized areas available in electronics for further study.

Very Large Scale Integration (VLSI) system design is the process of creating complex integrated circuits by combining million/billion number of transistors into a single chip. This programme aims to prepare the students to design analog and digital integrated circuits using custom and semicustom design flow.

Worldwide, for the past five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The improvement of integration level, cost, speed, power, compactness and functionality of the integrated circuits leads to significant improvement in economic productivity and overall quality of life through proliferation of computers, communication, industrial and consumer electronics.

The improvement and complexity of VLSI system can be achieved by revolution of CMOS transistors, miniaturization of transistors, VLSI design methodology, EDA tool support, fabrication support, new design idea and innovative technology which are active research area in VLSI system design.

The ICs/Micro Processor/Micro-Controller/ chips developed and fabricated using VLSI technology become the heart of embedded systems. Embedded systems have become pervasive across various domains such as automotive, industrial and communication systems leading to tremendous growth in the application and innovation of networked and high performance real time embedded systems.

To sustain the growth rate, the organizations involved in VLSI technology and Embedded Systems development are in need of designers, analysts, developers, manufacturing, testing and marketing engineers as well as managers with a postgraduate degree in VLSI design and Embedded System sector.

The **School of Electronics and Communication Engineering at REVA UNIVERSITY** offers M. Tech., in **VLSI and Embedded Systems**–a postgraduate programme to create motivated, innovative, creative and thinking graduates to fill the roles of Electronic Engineers who can conceptualize, design, analyze and develop VLSI and Embedded systems to meet the modern day requirements.

The number of product and service based semiconductor industry are growing, thus various career opportunities exist in product development companies including mobile and consumer electronics, computing, telecommunications, networking, data processing, automotive, healthcare and industrial applications.

In this context**, The School of Electronics and Communication Engineering at REVA UNIVERSITY would like to add to the growing human resources needs of VLSI and Embedded system sector as engineers through its M. Tech. programme in VLSI and Embedded Systems.**

During the programme the theoretical foundation is built through courses like Digital VLSI design, High speed VLSI design, Low power VLSI Design, Analog and mixed mode design, system on chip design. The practice includes skill development in both Front end & Back end designs, verification and testing. The program also offers strong knowledge and practical skills in developing embedded solutions on varied platforms such as FPGA, Advanced microcontrollers and processors. The students learn to implement real time embedded systems. The designers gain practical knowledge through mini and major projects in both VLSI and Embedded system design domains.

Programme Educational Objectives (PEOs)

The aim of the programme is to produce postgraduates with advanced knowledge and understanding of VLSI and Embedded Systems; higher order critical, analytical, problem solving and transferable skills; ability to think rigorously and independently to meet higher level expectations of electronics industry, academics, research establishments or take up entrepreneurial route.

Program Educational Objectives (PEO's)

The programme educational objectives of the Electronics and Communication Engineering of REVA University is to prepare graduates

PEO-1	To have successful professional careers in national and multinational organization and communicate effectively as a member of a team orto lead a team.
PEO-2	To continue to learn and advance their careers throughactivities such asresearch and development, acquiring doctoral degree, participation in national level research programmes, teaching and research at university level etc.,
PEO-3	To be active members ready to serve the society locally and internationally, may takeupentrpreneurship for the growth of economy and to generate employment; and adopt the philosopy of lifelong learning to be aligned with economic and technological development.

Program Outcomes (POs)

After successful completion of the programme, the graduates shall be able to

PO1. **Demonstrate in-depth knowledge** of VLSI and Embeded Systems, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO2. **Analyze complex engineering problems critically**, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

PO3. **Think laterally and originally, conceptualize and solve engineering problems, evaluate** a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO4. **Extract information pertinent to unfamiliar problems through literature survey and experiments**, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

PO5. **Create, select, learn and apply appropriate techniques**, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

PO6. **Possess knowledge and understanding of group dynamics, recognize** opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO7**. Demonstrate knowledge and understanding** of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors.

PO8. **Communicate with the engineering community, and with society at large**, regarding **complex engineering activities** confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO9: **Recognize the need for**, and have the preparation and ability to engage in **life-long learning** independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10. **Acquire professional and intellectual integrity,** professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11. **Observe and examine critically the outcomes** of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback (**SELF learning**)

Programme Specific Outcomes (PSO's)

After successful completion of the programme, the graduates shall be able to

1. Isolate and solve complex problems in the domains of VLSI and Embedded Systems using latest hardware and software tools and technologies, along with analytical and managerial skills to arrive at cost effective and optimum solutions either independently or as a team.
2. Implant the capacity to apply the concepts of FPGA, ASIC, System On Chip, IoT and cyber physical systems, etc. in the design, development and implementation of application oriented engineering systems
3. Design, Model, Analyze and VLSI and Embedded Systems to solve real life and industry problems.

REVA UNIVERSITY
Bengaluru, India

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

M. Tech. VLSI & Embedded Systems- Part Time

Scheme of Instructions (effective from Academic Year 2019-2022)

Sl No	Course Code	Title of the Course	HC/ SC	Credit Pattern			
				L	T	P	Total
FIRST SEMESTER							
1	M18VP1010	Advanced Mathematics	HC	4	1	0	5
2	M18VP1020	CMOS VLSI Design (I)	HC	4	0	1	5
3	M18VP1031	Advanced Digital System Design using Verilog	SC1	4	1	0	5
	M18VP1032	Semiconductor Device Modeling & Technology		4	1	0	5
	M18VP1033	Internet of Things- Practical Approach		4	1	0	5
		Total Credits					**15**
SECOND SEMESTER							
1	M18VP2010	Advanced Embedded System Design (I)	HC	4	0	1	5
2	M18VP2020	Design of Analog CMOS Integrated Circuits (I)	HC	4	0	1	5
3	M18VP2031	Unix/Linux Shell Scripting and Python Basics	SC2	4	1	0	5
	M18VP2032	SOC Design		4	1	0	
		Total Credits					**15**
THIRD SEMESTER							
1	M18VP3010	Real Time Operating Systems (I)	HC	4	0	1	5
2	M18VP3021	Low Power VLSI Design	SC3	4	1	0	5
	M18VP3022	VLSI for Signal Processing		4	1	0	
	M18VP3031	High Speed VLSI Design	SC4	4	1	0	5

3	M18VP3032	ASIC Design and Verification with SystemVerilog		4	1	0	
		Total Credits					**15**
FOURTH SEMESTER							
1	M18VP4011	MSP430 (I)	SC5	4	0	1	5
	M18VP4012	FPGA Based Embedded System Design (I)		4	0	1	5
	M18VP4013	Synthesis and Optimization of Digital Circuits(I)		4	0	1	5
	M18VP4014	CMOS RF Circuit Design(I)		4	0	1	5
	M18VP4015	Advances in VLSI Design (I)		4	0	1	5
2	M18VP4021	MEMS	SC6	4	1	0	5
	M18VP4022	Advanced Computer Architecture(I)		4	0	1	5
		Total Credits					**10**
FIFTH SEMESTER							
1	M18VP5010	MOOC / Swayam / Edx / Harvard / CM / Internship/Soft skill training	-	0	0	3	3
2	M18VP5020	Sports, Yoga, Music, Dance, Theatre	RULO	0	0	2	2
3	M18VP5030	Mini Project	HC	0	0	9	9
4	M18VP5040	Automotive Electronics	OE	3	1	0	4
		Total Credits					**18**
SIXTH SEMESTER							
1	M18VP6010	Project work and Dissertation	HC	0	2	20	20
2	M18VP6020	MOOC / Swayam / Edx / Harvard / CM /	RULO	-	0	0	3
		Total Credits					**23**
	Total Credits for four Semesters						**96**

Note: HC = Hard Core: SC= Soft Core

M.Tech. (VLSI & Embedded Systems – Part Time)Programme

Detailed Syllabus

(Effective from Academic Year 2018)

Semester – I:

Course Code	Course Title	Course Type	L	T	P	C
M18VP1010	Advanced Mathematics	HC	4	1	0	5

Prerequisites:

1. Basic knowledge of matrix mathematics and linear transformations.
2. Linear and parabolic partial differentiation and scalar wave equation in one space dimension.
3. Basics of Laplace transforms, Fourier transforms and Poisson equation by Fourier transform.
4. Simplex algorithm and nonlinear programming.

Course Objectives:

1. To understand the advanced concepts in Matrix theory and calculus.
2. To Study the numerical, analytical and logical problem solving using transform methods.
3. To learn applications of Poisson and Fourier transform methods.
4. To understand the concept of elliptic equation.
5. To study the various algorithms in linear and nonlinear programming.

Course Outcomes:

On completion of this course the student will be able to:

1. Identify and describe different techniques in solving Engineering problems using Matrix method.
2. Describe the Euler equation of first and higher order degree.
3. Apply Laplace transform to one dimensional wave.
4. Analyse properties of harmonic functions.
5. Present the concepts Two Phase and Big M techniques.
6. Explain problem solving using Lagrange's multiplier method.

Mapping of Course Outcomes with programme Outcomes

Course Code	POS/ COs	P O1	P O2	P O3	P O4	P O5	P O6	P7	P O8	P O9	PO 10	PO 11	PS O1	PS O2	PS O3
M18VP10 10	**CO1**	**3**	**2**	**3**	**4**					**3**			**1**	**1**	**2**
	CO2	**3**	**3**	**2**	**1**				**2**					**2**	**1**
	CO3	**1**	**3**	**2**	**1**					**1**					
	CO4	**2**	**3**	**1**	**2**										
	CO5	**3**	**3**	**2**	**1**				**2**					**2**	**1**
	C06	**3**	**3**	**2**	**1**				**2**					**2**	**1**

Course Contents:

Unit 1: Matrix Theory, Calculus of Variations

QR EL Decomposition – Eigen values using shifted QR algorithm- Singular Value EL Decomposition - Pseudo inverse- Least square approximations

Concept of Functional- Euler's equation – functional dependent on first and higher order derivatives – Functional on several dependent variables – Isoperimetric problems- Variation problems with moving boundaries.

Unit 2: Transform Methods

Laplace transform methods for one dimensional wave equation – Displacements in a string – Longitudinal vibration of an elastic bar – Fourier Transform methods for one dimensional heat conduction problems in infinite and semi-infinite rod.

Unit 3: Elliptic Equation

Laplace equation – Properties of harmonic functions – Fourier transforms methods for Laplace equations. Solution for Poisson equation by Fourier transforms method.

Unit 4: Linear and Non Linear Programming

Simplex Algorithm- Two Phase and Big M techniques – Duality theory- Dual Simplex method. Non Linear Programming –Constrained external problems- Lagrange's multiplier method- Kuhn- Tucker conditions and solutions.Recent trends in the related areas from journals, Conference proceedings Book chapters.

References:

1. Richard Bronson, "**Schaum's Outlines of Theory and Problems of Matrix Operations**", McGraw-Hill, 1988.
2. Venkataraman M. K., "**Higher Engineering Mathematics**", National Publications Co., 1992.
3. Elsgolts, L., "**Differential Equations and Calculus of Variations**", Mir, 1977.
4. Sneddon, I.N., "**Elements of Partial Differential Equations**", Dover Publications, 2006.
5. SankaraRao, K., "**Introduction to Partial Differential Equations**", Prentice – Hall of India,1995.
6. Taha H A, "**Operations Research - An Introduction**", McMilan Publishing co, 1982.

Course Code	Course Title	Course Type	L	T	P	C
M18VP1020	CMOS VLSI Design	HC	4	0	1	5

Prerequisites:

1. Working principle of MOS transistor theory and MOSFET characteristics.

2. Static characteristics, transient response and propagation delay calculations of MOS inverters.
3. Basic principles of pass transistor circuits and dynamic CMOS characteristics.
4. Basics of volatile memory and non volatile memory and low power CMOS logic circuits.
5. Knowledge on BiCMOS and BJT theory.
6. Concept of electrostatic discharge (ESD) and basics of latch up prevention and process variations.

Course Objectives:

1. To understand an overview of working principle of MOS transistor and MOS inverters.
2. To be acquainted with all the definitions associated with MOS inverters.
3. To understand dynamic logic circuits.
4. To get understand of semiconductor memory.
5. To study chip input output devices.

Course Outcomes:

On completion of this course the student will be able to:

1. Explain the working principle of MOS transistor and MOS inverters.
2. Define all the definitions associated with MOS inverters.
3. Analyse dynamic logic circuits.
4. Describe the semiconductor memory.
5. Explain chip input output devices.

Mapping of Course Outcomes with programme Outcomes

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
M18VP1020	CO1	3	2		2		1	1			2		3		3	2
	CO2	3	3	3			1			2			2		3	2
	CO3	3	3				2			1			1		3	2
	CO4	3	3			2							1		3	2
	CO5	3	2		2		1	1			2		3		3	2

Course Contents:

Unit 1: MOS Transistor, MOS Inverters

The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, And MOSFET Scaling and Small-Geometry Effects.

Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter.

Unit 2: MOS Inverters (continued)

Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, and Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, and Switching Power Dissipation of CMOS Inverters.

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Unit 3: Semiconductor Memories

Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). Low-Power CMOS Logic Circuits: Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits.

BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Unit 4: Chip Input and Output (I/O) Circuits

Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Design for Manufacturability : Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling, Parametric Yield Estimation, Parametric Yield Maximization, Worst-Case Analysis, Performance Variability Minimization.

Recent trends in the related areas from journals, Conference proceedings Book chapters.

References:

1. Sung Mo Kang and YosufLeblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition, 2003.
2. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

CMOS VLSI Lab

Course Objectives:

1. To understand the ASIC Design flow
2. To demonstrate VLSI CAD tool- Cadance
3. To desing VLSI Digital Circuits
4. To perform Area, power and timing analysis of the designed digital circuits.

Course Outcomes:

On completion of this course the students will be able to:

1. Design the digital VLSI circuits
2. Perform the Power, area and timing analysis of the designed digital circuits

Mapping of Course Outcomes with programme Outcomes

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	P O 10	P O 11	P O 12	PSO 1	PSO 2	PSO 3
M18VP1020	CO1	3	3				2			1			1		3	2
	CO2	3	2		2		1	1			2		3		3	2

Lab Experiments

1. Write a VHDL/Verilog code to realize the A Buffer. Simulate & synthesize the same on FPGA kit.
2. Write a VHDL/Verilog code to realize the inverter. Simulate & synthesize the same on FPGA kit.
3. Write a VHDL/Verilog code to realize the Transmission Gate. Simulate & synthesize the same on FPGA kit.
4. Write a VHDL/Verilog code to realize the universal gates Simulate & synthesize the same on FPGA kit..
5. Write Verilog / VHDL Code for the following circuits and their Test Bench for **verification**, observe the waveform and **synthesis** the code with technological library with given Constraints.
    a. RS Flip flop
    b. D Flip flop
    c. JK Flip flop
    d. T Flip flop
    e. Master Slave JK Flip flop
6. Write Verilog / VHDL Code for the Serial & Parallel adderand their Test Bench for **verification**, observe the waveform and **synthesis** the code with technological library with given Constraints.
7. Write a VHDL/Verilog code to realize the kit 4-bit counter [Synchronous and synchronous counter] Simulate & synthesize the same on FPGA kit.
8. Write a VHDL/Verilog code to realize l the kit Successive approximations register [SAR]. Simulate & synthesize the same on FPGA.
9. Mini Project*

M18VP1031	Advanced Digital System Design using Verilog	SC	4	0	1	5

Pre Requisites:

Knowledge on Digital system design, Boolean algebraic theorems and number systems, Basics of sequential logic and memory types, Principles of ICs, PLDs and interfacing memory.

Course Objectives:

This course will enable students to:

1. Understand the concepts of Verilog Language.
2. Design the digital systems as an activity in a larger systems design context.
3. Study the design and operation of semiconductor memories frequently used in application specific digital system.
4. Illustrate the different components and functions related to design of Combinational circuits.
5. Illustrate the different components and methodology related to design of Sequential circuits.
6. Provide an Understanding to concepts FSM basics.

Course Outcomes:

After studying this course, students will be able to:

1. Design & Construct the combinational circuits using discrete gates and programmable logic devices.
2. Describe Verilog model for sequential circuits and test pattern generation.
3. Apply different modeling techniques in the programming of Verilog HDL
4. Explore the different types of semiconductor memories and their usage for specific chip design.
5. Understand and analyze the programming of combinational and sequential logic design in Verilog HDL
6. Design and synthesis of different types of processor and I/O controllers that are used in embedded system design.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
	CO1	4	4	3	3	2							1	1		2
	CO2	1	4	3	3	2							2	1		2

M18 VP1031	**CO3**	**4**	**3**	**4**	**2**	**2**					**1**		**1**	**1**		**2**
	CO4	**1**	**3**	**4**		**2**							**1**	**1**		**2**
	CO5	**4**	**4**	**3**	**3**	**2**							**1**	**1**		**2**
	CO6	**1**	**4**	**3**	**3**	**2**							**2**	**1**		**2**

Unit 1: Introduction to Digital System and Methodology

Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Design Methodology.

Gate-level combinational circuit:Introduction, General description, Basic lexical elements and data types, Data types, Program skeleton, Structural description, Test bench.

Overview of FPGA and EDA software:Introduction, Architecture of FPGA, Development flow, HDL for combinational Circuits, Design of Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter.

Unit 2: Functions tasks and User defined Primitives

Introduction, functions, tradeoff between hardware and speed, scope of functions, recursive functions, tasks, task definition, task enabling, user defined primitives, combinational UDPs, More general combinational UDPs, Instantiation of UDP, Combinational UDP and Function, Sequential UDPs, UDP instantiation with delays, vector type instantiation of UDP

Unit 3: Sequential Basics:

Storage Elements, Flip-flops and Registers, Shift Registers, Latches, Sequential Data paths and Control, Finite-State Machines, Clocked Synchronous Timing Methodology, Asynchronous Inputs, Verification of Sequential Circuits, Asynchronous Timing Methodologies,

Memories: General Concepts Memory Types, Asynchronous Static RAM Synchronous Static RAM, Multiport Memories, Dynamic RAM, Read - Only Memories.

Unit 4: Queues, PLAS, Compiler directives and FSMS:

File based tasks and functions, compiler directives, time related tasks, queues, PLDs, programming PLD in Verilog, Design of finite state machine- Moore machine, Melay machine.

Text Books:

1. T.R. Padmanabhan, B. Bala Tripura Sundari , Design through Verilog HDL", Wiley Publication.
2. Pong P Chu, "FPGA Prototyping by Verilog Examples", Wiley, 2006.

References:

1. Peter J. Ashenden, **"**Digital Design: An Embedded Ssytems Approach Using VERILOG", Elesvier, 2010.
2. Frank Vahid, "Digital Design", Wiley, 2006.

Course Code	Course Title	Course Type	L	T	P	C
M18VP1032	Semiconductor Device Modeling &	SC	4	1	0	5

Prerequisites:

1. Basic knowledge of Electronics Devices.

Course Objectives:

1. Understand the basic concepts of semiconductor materials
2. Characterize the concepts of P- N Junction diode
3. Understand the basic characteristics of metal semiconductor junction
4. Study the device modeling

Course Outcomes:

On completion of this course the student will be able to:

1. Analyze the concepts of semiconductor materials and analyze its properties
2. Analyze the characteristics and concepts of P-N Junction Diode
3. Analyze the characteristics and concepts of Metal-Semiconductor Junction
4. Analyze the characteristics and concepts of MOSFET and BJT
5. Apply, Awareness and Understanding of current trends in semiconductor device modeling in Design and Fabrication Unit

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	P0 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
M18VP 1032	CO1	3		2	1									3	1	2
	CO2	2		3	1									2	1	3
	CO3	1		3	2									1	2	3
	CO4	3		1	2									1	3	2
	CO5	3		2	1									3	1	2

Course Contents:

Unit 1: Semiconductor Materials

Intrinsic carrier concentration: Dopant atoms and energy levels, Ionization energy: the extrinsic semiconductor, Position of Fermi-energy level, variation of EF with doping concentration and temperature. Carrier drift: mobility, conductivity and velocity saturation, Carrier Diffusion: diffusion current density, total current density, The Einstein relation, Excess carrier generation and recombination, Characteristics of excess carriers – continuity equation and time-dependent diffusion equation.

Unit 2: PN Junction diode

Basic structure, built-in potential, electric field, space charge width, reverse applied bias space charge width and Electric field, junction capacitance, Ideal current-voltage relationship, minority carrier distribution, Ideal PN-junction currents under forward and reverse bias, Temperature effects, small signal model of PN-junction, Equivalent circuits, recombination current, junction breakdown; SPICE models of p-n diode.

Unit 3: Metal Semiconductor Junction and FET Capacitor

Schottky barrier, I-V and C-V characteristics of M-S junction, thermal emission and tunneling current, Field-Effect Transistors: JFET- current-voltage characteristics, effects in real devices, high-frequency and high-speed issues. MOS structure: Energy band diagrams, work function difference, Depletion layer thickness, Flat band voltage, threshold voltage, charge distribution, MOS Capacitance – voltage characteristics.

Unit 4: Bipolar Transistor and Current trends

Basic Principle of Operation: Simplified transistor current relationship, Modes of operation, amplification with bipolar transistors, Minority carrier distribution, Forward active mode and other modes of operation, Low frequency common base current gain, Non-ideal effects – Base width modulation, breakdown voltage, equivalent circuit models, Eber's – Moll model, Hybrid – pi model, Frequency limitation, large signal switching; SPICE models of BJT.

References:

1. N. DasGupta, and A. DasGupta, Semiconductor Devices: Modelling and Technology, Prentice Hall of India Private Limited, New Delhi, 2004.
2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 5th edition, Prentice Hall of India Private Limited, New Delhi, 2000.
1. Chenming Calvin Hu, Modern Semiconductor Devices for Integrated Circuits, Pearson, 2009.
2. Y. Taur, and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University press, 1998
3. S. M. Sze, VLSI Technology, 2nd edition, McGraw-Hill, 1998
4. S. K. Dieter, Semiconductor Material and Device Characterization, by John Wiley and Sons, New York, 1990.
5. G. W. Roberts and A. S. Sedra SPICE 2nd edition, Oxford University Press, 1997
6. Yuan TaurandTak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press; 2 edition, 2013.

Course Code	Course Title	Course Type	L	T	P	C
M18VP1033	Internet of Things- Practical Approach	**SC**	**4**	**1**	**0**	**5**

Prerequisites:

Basics of wireless networks, protocols, sensors

Course Objectives:

1. To introduce the full connected-product experiences by integrating Internet services and physical objects
2. To give an insight into developing prototypes of Internet-connected products using appropriate tools
3. To introduce theBasicArduino programming. Extended Arduino libraries. Arduino-based Internet communication
4. To provide insghtintoXML and JSON, HTTP APIs for accessing popular Internet services

Course Outcomes

On completion of this course the student will be able to:

1. Understand full connected-product experiences by integrating Internet services and physical objects
2. Analyzing, designing, and developing prototypes of Internet-connected products using appropriate tools.
3. Identifying, classifying and describing different kinds of Internet-connected product concepts Describe different network protocols
4. Analyzing the challenges and applying adequate patterns for user-interaction with connected-objects

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
M18VP1033	**CO1**	**1**				**2**	**3**							**3**	**1**	**2**
	CO2	**2**	**1**			**2**	**3**							**2**	**1**	**3**
	CO3	**1**				**2**	**3**							**3**	**2**	**1**
	CO4	**1**				**2**	**3**									

Course Contents:

Unit 1: Introduction to the Internet of Things

Origins.Early concepts and products.Examples of current products and value propositions. Architectures and design patterns. Analysis of a full connected-object experience.State of the Art, challenges and future directions.

Unit 2: Prototyping Connected Objects

Open-source prototyping platforms.Basic Arduino programming.Extended Arduino libraries.Arduino-based Internet communication. Practical activities

Unit 3: Integrating Internet Services

XML and JSON. HTTP APIs for accessing popular Internet services (Facebook, Twitter, and others). Practical activities

Unit 4: Project Development and Competition

Development of a project including: value proposition, physical connected object prototyping, programming the behaviour, accessing Internet services and designing the user experience. Case studies

Reference books:

1. Smart Things: Ubiquitous Computing User Experience Design. Mike Kuniavsky. Morgan Kaufmann Publishers. 2010
2. Meta Products: Building the Internet of Things. Sara Cordoba, WimerHazenberg, Menno Huisman. BIS Publishers. 2011.
3. Getting Started with Arduino (Make: Projects). Massimo Banzi. O'Reilly Media. 2008
4. Emotional Design: Why We Love (or Hate) Everyday Things. Donald A. Norman. Basic Books, 2004.
5. Physical Computing: Sensing and Controlling the Physical World with Computers. Tom Igoe, Dan O'Sullivan. Premier Press. 2004.

Semester – II:

Course Code	Course Title	Course Type	L	T	P	C
M18VP2010	Advanced Embedded Systems Design	HC	4	0	1	5

Prerequisites:

1. Concept of Embedded systems and its design optimization.
2. Knowledge on architecture of embedded systems and embedded microcontroller cores.
3. Working principle of interfacing subsystems and external systems and DSP.
4. Concepts of real time programming and RTOS.

Course Objectives:

1. Understand how to design an embedded system.
2. To know how to partition a system to hardware and software parts efficiently.
3. To know Hardware/software Co-design concepts.
4. To Understand the Architecture and Working of ARM Cortex-M3 Processors and Controllers.
5. To study the concepts of Architectural Support for High level languages.
6. To study the concepts of Architectural support for system Development and Operating systems.

Course Outcomes:

On completion of this course the students will be able to:

1. Design embedded system architectures for various applications.
2. Implement, Identify, formulate, and solve engineering problems.
3. Analyze and Compare various Processor and Controller Architectures with ARM
4. To identify different functional blocks in an ARM Microcontroller and their Applications
5. Program ARM Cortex-M3 MCUs by identifying the software development tools

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
M18VP 2010	CO1	3	3	3		2				2	3		3	2	3	2
	CO2	3	3	3		2				2	3		3	2	3	2
	CO3	3	3	3		2				2	3		3	2	3	2
	CO4	3	3	3		2				2	3		3	2	3	2
	CO5	3	3	3		2				2	3		3	2	3	2

Course Contents:

Unit 1: Introduction

Overview of embedded systems, embedded system design challenges, common design metrics and optimizing. Survey of different embedded system design technologies & trade-offs. Embedded microcontroller cores, embedded memories, Examples of embedded systems.Architecture for embedded system.

Unit 2: Introduction to Cortex-M3 Processor

A Brief History, Architecture Versions, Different MCU architectures vs ARM, ARM Processor Families, Cortex-M3 Processor Applic Interrupt/Exception Sequences, Nested Interrupts, Tail-Chaining, Late Arrivals, Interrupt Latency, Exception/Interrupt Handlers, Software Interrupts

Unit 3: Cortex-M3Programming

Typical Development Flow, Development Tools – C Compilers and Debuggers, Embedded OS Support, Embedded C Programming using Keil MDK-ARM

Cortex Microcontroller Software Interface standard (CMSIS) – Areas of standardization, Organization and using CMSIS, Overview of NxP's LPC1768, Memory map, Understanding different functional blocks and their Applications in LPC 1768 - System Control, Clocking and Power Control, Timers, WDT, RTC, ADC, I2C, SPI

Unit 4: Cortex-M3MicrocontrollersProgramming and Development

Pin Connect block, GPIO Programming, Configuring GPIOs for External Interrupts. Understanding UART and its Applications, Configuration for Serial Communication.

References:

1. Jack Ganssle, "**The Art of Designing Embedded Systems**", Elsevier, 1999.
2. J.W. Valvano, "**Embedded Microcomputer System: Real Time Interfacing**", Brooks/Cole, 2000.
3. David Simon, "An Embedded Software Primer", Addison Wesley, 2000.
4. Gomaa, "**Software Design Methods for Concurrent and Real-time Systems**", Addison-Wesley, 1993.
5. InstructorReferenceMaterial
6. JosephYiu, "THE DEFINITIE GUIDE TOTHE ARMCORTEX-M3"
7. ManualsandTechnicalDocumentsfromthe ARM Inc, web site.

Advanced Microcontroller Lab

CourseObjectives:

The objective of the course is:

1. To Learn CProgramming, DebuggingandInterfacingPeripherals fora given ARM Cortex-

M3 Microcontroller

Course Outcomes:

Thestudents willbe ableto

1. ProgramARM Cortex-M3 MCUTargetusingKeiluVisionIDE
2. Interfaceand Programhardware peripherals like LED,Push Button Switch, LCD,Keypad
3. Establish serialcommunicationbetweentheMCU targetand Desktop PC.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
M18VP 2010	**CO1**	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO2	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO3	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**

Laboratory Experiments

1. InterfaceanExternalPushButtonSwitch,LED,withMCUtargetboard,andWriteaCProgram to Configure and Controlthe ON-OFF operation ofthe LEDusingtheswitch. (*Configure Switchas an Externalinterruptsource*)
2. Interfacea4x4MatrixKeypad,LEDsArray,withMCUtargetboard, and WriteaCprogramto displaythebinaryequivalentpattern ofthe numeric keypressedon theLEDsarray.
3. Interfacea16x2LCDforits4-bitmodeoperation,withMCUtargetboardandWriteaC Programto displaya message on boththelinesof theLCD.
4. WriteaCProgramtoConfiguretheon-chipUARTfunctionalblockoftheMCUtargetboardto outputa messageon serialterminalofa hostmachine via itsserial/ COM port.

Course Code	Course Title	Course Type	L	T	P	C
M18VP2020	Design of Analog CMOS Integrated Circuits	HC	4	0	1	5

Prerequisites:

1. Basics of MOS devices and its characteristics.
2. Concepts of single stage amplifiers and frequency response of amplifiers.
3. Knowledge on differential amplifiers, Operational amplifiers and current mirrors.
4. Basic knowledge on DAC and ADC architectures and phase locked loops.

Course Objectives:

1. To understand the basics and operation of MOS devices.

2. To analyse and understand analog CMOS integrated circuits.
3. To analyse and design single stage MOS amplifier circuits.
4. To understand the basic operation of differential amplifier and op-amps.

Course Outcomes:

On completion of this course the student will be able to:

1. Design single stage, differential and current mirror
2. Analyse the stability, feedback in amplifiers, op-amps
3. Design oscillators and PLL.
4. Design ADCs and DACs

Mapping of Course Outcomes with Program Outcomes

Course Code	POs/ COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO1	PSO2	PSO3
M18VP2020	**CO1**	**3**	**2**	**3**	**1**								**2**	**1**	**3**
	CO2	**3**	**3**	**2**	**1**								**1**	**2**	**3**
	CO3	**2**	**2**	**3**	**2**								**3**	**1**	
	CO4	**2**	**1**	**2**	**1**								**2**	**3**	

Course Contents:

Unit 1: Basic MOS Device Physics

General considerations, MOS I/V Characteristics, second order effects, MOS device models. Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models**.**

Unit 2: Differential Amplifiers & Current Mirrors

Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors.

Operational Amplifiers: One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps.

Unit 3:Oscillators and Phase Locked Loops

Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. Band gap References and Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, and Switched Capacitor Amplifiers.

Unit 4:Data Converter Architectures

DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

References:

1. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
2. Philip Allen and Douglas Holberg, "CMOS Analog Circuit Design", Oxford University, Press, 2011.
3. R. Jacaob Baker, Harry W Li and David E Boyce, "CMOS Circuit Design, Layout, Stimulation", CMOS Circuit PHI Edn, 2005.

Design of Analog CMOS Integrated Circuits Lab

Course Objectives:

1. Learn the CAD tool and the flow of the Full Custom IC design cycle.
2. Design the various analog CMOS VLSI circuits.
3. Perform DRC, LVS and Parasitic Extraction of the various designs.

Course Outcomes:

1. Demonstrate the VLSI Cad tool to design CMOS VLSI analog circuits
2. Design, implement and analyse various Analog mixed mode circuits
3. Perform DRC, LVS for the designed circuits.
4. Carry out the mini project on the design of a CMOS subsystem.

Mapping of Course Outcomes with Program Outcomes

Course Code	POs/ COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO1	PSO2	PSO3
M18VP2020	CO1	3	2	3	1								2	1	3
	CO2	3	3	2	1								1	2	3
	CO3	2	2	3	2								3	1	
	CO4	2	1	2	1								2	3	

Lab Experiments

1. Design of inverter with given specifications, and perform the following
    1. Draw the schematic and perform
        a. DC analysis
        b. Transient Analysis
    2 Draw the Layout and perform DRC and ERC
    3. Extract RC and Back annotate the same and verify the design
2. Design the following circuits with given specifications*, completing the design flow mentioned below:
    a.Draw the schematic and verify the following
    i) DC Analysis
    ii) AC Analysis
    iii) Transient Analysis
    b.Draw the Layout and verify the DRC, ERC, LVS

c.Extract RC and back annotate the same and verify the Design.

i) A Single Stage differential amplifier
ii) Common source amplifier
iii) Design an op-amp with given specification

Course Code	Course Title	Course Type	L	T	P	C
M18VP2031	Unix/Linux Shell Scripting and Python Basics	SC	4	1	0	5

Prerequisites:
Basic knowledge of Unix OS.

Course Objectives:

1. Understand the and write the shell scripts
2. Understand the concept of process in Unix
3. Study the basic concepts of python scripting language

Course Outcomes:
On completion of this course the student will be able to:

1. Design scripting code for a given application
2. Apply various conditional statements, loops and command line arguments to develop the script code
3. Develop the python scripting code

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	P0 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	P O 10	P O 11	P O 12	PSO 1	PSO 2	PSO 3
M18VP 2031	CO1		2	1		3								3	1	2
	CO2	2	1		2	3								2	1	3
	CO3	1		2		3								3	2	1

Course Contents:

Unit 1: Shell Basics, Writing first script

Types of shells, Shell functionality, Environment, Writing script & executing basic script, Debugging script, Making interactive scripts, Variables (default variables), Mathematical expressions,

Conditional Statements and Loops: If-else-elif, Test command, Logical operators-AND,OR,NOT, ase –esac, Loops, While, For, Until, Break & continue.

Unit 2: Command line arguments

Positional parameters, Set & shift, IFS, Break & continue, Processing file line by line Functions, What is regular expression, Grep, cut, sort commands, Grep patterns.

Unit 3:SED & AWK, Processes

Concept of process in Unix, Background processes, Scheduling processes -At, batch &Cron

Unit 4: Python Basic

Latest developments in the semiconductor device modeling and introduction to device simulation tools & technologies, e.g., Silvaco-CMOS Process and Smart SPICE.Exposure to equipment and process used in Semiconductor Fab.Unit, Test and Measure Equipments.

References:

1. Brian W. Kernighan & Rob Pike, The Unix Programming Environment, Prentice Hall of India Private Limited, New Delhi, 2004.
2. Carl Albing, JP Vossen, and Cameron Newham,BashCookbook,O'Reilly 2007.
3. Tim Hall and J-P Stacey,Python 3 for Absolute Beginners, Apress, 2009.

Course Code	Course Title	Course Type	L	T	P	C
M18VP2032	SOC Design	SC	4	1	0	5

Prerequisites:

1. Basics of SoC design and system architecture.
2. Concepts of interconnect architecture and bus architecture of Soc.
3. Principles of memory design and cache architecture.
4. Basic knowledge of ASIC design flow and FPGA design flow.

Course Objectives:

1. Provide a comprehensive introduction to the ASIC and SoC technology.
2. Provide theoretical and practical aspects of ASIC and SoC design.
3. Introduce ASIC design, ASIC library design and Programmable ASIC.
4. Give an overview to SoC design, its challenges and Design flow.
5. To understand the memory design concepts in processors.
6. To understand ASIC design flow using semi/full /standard cells.

Course Outcomes:

On completion of this course the students will be able to:

1. Select the appropriate processors for a given application keeping area, power and speed as constraints and to Deepen CMOS VLSI design knowledge
2. Design full custom/ semicustom/ standard cells for ASIC

3. Implement network on chip technologies
4. Analyze memories using reconfigurable architectures for rapid prototyping
5. Analyze system on chip and board based systems.

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
M18VP 2032	CO1		2	1		3								3	1	2
	CO2	2	1		2	3								1	3	2
	CO3	1		2		3								2	3	1
	CO4		2	1		3								3	1	2
	CO5	2	1		2	3								1	3	2

Course Contents:

Unit-1: System Approach and Chip Basics

System Architecture, Components of the System, Hardware and Software. An approach for SoC Design, System On Chip Design Process: A canonical SoC Design, SoC Design flow - waterfall vs spiral, Top-down vs Bottom up, System Architecture and Complexity. Chip Basics. Cycle Time, Die Area and Cost, Ideal and Practical Scaling, Power, Area–Time–Power Trade-Offs in Processor Design, Reliability, Configurability.

Unit-2: Processors and Interconnects

Processor Selection for SoC, Basic Concepts in Processor Architecture, Instruction Handling, and Buffers, Minimizing Pipeline Delays, Branches. Vector, Very Long Instruction Word (VLIW), and Superscalar with case studies. Interconnect architectures for SoC. Bus architecture. Network on Chip topologies.Routing, Switching and Flow Control in NoCs.

Unit-3:Memory Design

System-on-Chip and Board-Based Systems – Scratchpads and Cache Memory, Basic Notions, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Cache, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SoC (On-Die) Memory Systems, Board-based (Off-Die) Memory Systems, Simple DRAM and the Memory Array, Models of Simple Processor–Memory Interaction.

Unit-4: ASIC Design

Full/Semi Custom with ASIC, Standard Cell based ASIC, Gate array based ASIC, Programmable logic device, FPGA design flow, ASIC cell libraries. ASIC Library Design, Logical effort and library cell design. Low-Level Design Entry, Schematic Entry, Hierarchical design, the cell library, connections, vectored instances and buses, Edit in place attributes, Net list, screener, back annotation.

Text Books:

1. Micheal J Flynn and Wayne Luk,"**Computer System Design: System-on-Chip**," Wiley, First Edition, 2011.
2. SudeepPasricha and NikilDutt,"**On-Chip Communication Architectures: System on Chip Interconnect**", Morgan Kaufmann, 2008.
3. Michael Keating, Pierre Bricaud, "**Reuse Methodology manual for System on chip designs**", Kluwer academic Publishers, 2nd edition-2008.
4. M.J.S .Smith, "**Application Specific Integrated Circuits**", Pearson Education, 2003.

Semester – III:

Course Code	Course Title	Course Type	L	T	P	C
M18VP3010	Real Time Operating Systems	HC	4	0	1	5

Prerequisites:

1. Concepts of Operating systems.
2. Basics of task management and task scheduling.
3. Knowledge on RTOS and memory management.
4. Basic knowledge on performance metrics and RTOS tools.

Course Objectives:

1. To acquire knowledge aboutconcepts related to OSsuch asSchedulingtechniques,threads, inter-threadcommunications, memorymanagement.
2. To acquire knowledge aboutdifferent typesofschedulingalgorithms
3. To studyaboutFreeRTOS
4. To understandthe various functionsofRTOS

Course Outcomes:

On completion of this course the students will be able to:

1. Describe the fundamental concepts of RTOS
2. Develop programs for real time services, firmware and RTOS.
3. Develop programs formulate threaded applications on FreeRTOS

Mapping of Course Outcomes with Program Outcomes

Course Code	POs/ COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO1	PSO2	PSO3
M18VP3010	**CO1**	**3**	**2**	**3**	**1**								**2**	**1**	**3**
	CO2	**3**	**3**	**2**	**1**								**1**	**2**	**3**
	CO3	**2**	**2**	**3**	**2**								**3**	**1**	

Course Contents:

Unit 1: Real time systems and Resources

Real-TimeSystemsandResources: Brief history of Real Time Systems, A briefhistory of Embedded Systems,Requirementsof Embedded System,ChallengesinEmbeddedSystem.System Resources, ResourceAnalysis, Real-Time ServiceUtility.

ProcessingwithReal TimeScheduling: SchedulerClasses,PreemptiveFixedPriority Scheduling Policieswithtimingdiagrams,Rate Monotonicleastupperbound,NecessaryandSufficientfeasibility,Deadline –MonotonicPolicy, Dynamic prioritypolicies,Worstcase executiontime, Deadlockand livelock.

Unit 2: Real Time Operating Systems

Operating Systembasics,TheKernel and its subsystems, Kernel Space andUser Space, Kernel Architecture, Types of operating system, Task, process and Threads, Multi-Processing and Multitasking, Typesofmultitasking,TaskScheduling, Taskstates,Non-Preemptivescheduling, PreemptiveScheduling,RoundRobinScheduling,IdleTask,TaskCommunication, Task Synchronization,Thread Safe ReentrantFunctions.

Unit 3: Embedded Firmware Design, development andFree RTOS

Embedded Firmware DesignApproaches, Super-loop basedapproach, EmbeddedOperatingSystem basedapproach,Programming in Embedded C, Integrated developmentenvironment (IDE), Overview of IDEs forEmbedded SystemDevelopment.

Introduction to FreeRTOS,multitaskingon an LPC17xx Cortex-M3 Microcontroller, LPC17xx Portof FreeRTOS, Resources UsedbyFreeRTOS,TaskManagement,TaskFunctions,TaskPriorities, Idle task and taskhookfunction,Creation and Deletion of tasks.

Unit 4: Embedded Systemdesignwith Free RTOS

QueueManagement, Characteristicsofa Queue,Workingwith LargeData, InterruptManagement, Queues within an Interrupt ServiceRoutine, CriticalSections and SuspendingtheScheduler, Resource Management, MemoryManagement.

References:

1. InstructorReferenceMaterial
2. SamSiewert,"Real-Time Embedded SystemsAnd Components".
3. ShibuKV,"Introduction to Embedded System".
4. "Usingthe FreeRTOSRealTime Kernel" FromFreeRTOS.
5. ManualsandTechnicalDocuments fromtheARMInc, web site.

Real Time Operating System Lab

CourseObjectives:

1. To PerformMultithreadedProgrammingin RTOS Platform.
2. To AcquiretheKnowledgeonworkingofInterruptsand WritingISRs.

CourseOutcomes:

Thestudents willbe ableto

1. Programin Con FreeRTOSwin32 and ARM Cortex-M3 Port.
2. DemonstrateTaskManagement.
3. Demonstrate Inter-TaskCommunication.

Mapping of Course Outcomes with Program Outcomes

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P7	PO 8	PO 9	PO 10	PO 11	PSO 1	PSO 2	PSO 3
M18VP3010	CO1	3	2	3	1								2	1	3
	CO2	3	3	2	1								1	2	3
	CO3	2	2	3	2								3	1	

Laboratory Experiments

1. WriteaCProgramtoperformthetaskManagementinFreeRTOS,usingwin32portonVisual Studio IDE:
   a. CreateTwoTasksand Passthe"*Task-Name*"asanargument to thetaskfunction. b. Demonstrate the useofidletaskhookfunction.
   c. Updatethetaskprioritydynamically.

2. WriteaCProgramtocreateataskinFreeRTOS,usingwin32portonVisualStudioIDE;that periodically generatesasoftwareinterruptforevery1sec.

3. Writea C ProgramtoDemonstrate Inter-TaskCommunication usingQueues in FreeRTOS, use
   ARM Cortex-M3 Port (LPC1768 MCUKit)
   a. Task-1 createsdata(storesin a structure)andsendsitto the queue
   b. Task-2 readsthe message packetfromthe queue andreactsaccordingly.

4. WriteaCProgramtoDemonstrateTaskSynchronizationandResourceSharingamongmultiple tasks inFreeRTOS,useARM Cortex-M3 Port(LPC1768 MCU Kit)
   a. Assumemultipletasks tryingto write datato aserialport.
   b. UseMutexsemaphoreto gainexclusive accessto serialport.

Course Code	Course Title	Course Type	L	T	P	C
M18VP3021	Low Power VLSI Design	SC	4	1	0	5

Prerequisites:

Concepts of low power VLSI design and scaling technologies involved, Knowledge on simulation programming with integrated circuits and probabilistic power analysis, Basics of design parameters of low power circuits and low power architecture, Knowledge on clock distribution and architectural level methodologies.

Course Objectives:

This course will enable students to:

1. understand different sources of power dissipation in CMOS & MIS structure.
2. explore the different types of low power adders and multipliers.
3. focus on synthesis of different level low power transforms.
4. Analyze the various energy recovery techniques used in low power design.

Course Outcomes:

On completion of this course the student will be able to:

1. Analyse different source of power dissipation and the factors involved.
2. Understand the different techniques involved in low power adders and multipliers.
3. Understandings of the impact of various low powers transform
4. Identify and analyse the different techniques involved in low power design

Mapping of Course Outcomes with Program Outcomes:

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO10	PO11	PO12	PS O1	PS O2	PS O3
M18VP3021	**CO1**	**3**	**3**							**3**	**3**	**2**				
	CO2	**3**	**2**	**3**						**3**	**3**	**3**		**3**		**3**
	CO3	**3**	**3**							**3**	**2**	**3**				
	CO4	**3**	**3**							**2**	**1**	**3**		**3**		

Course Contents:

Unit 1: Introduction

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Impact of technology Scaling, Technology.

Unit 2: Power estimation, Simulation Power analysis

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Unit 3: Synthesis for low power and Low power Clock distribution

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation,

Clock distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

Unit 4: Algorithm and Architectural Level Power Analysis and Optimization

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Software design for Low power: Introduction, sources of software power dissipation, software power estimation, software power optimization- minimizing the memory access costs.

Text Books:

1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000.
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002.
3. Rabaey, Pedram, "**Low Power Design Methodologies**" Kluwer Academic, 1997.

Course Code	Course Title	Course Type	L	T	P	C
M18VP3022	VLSI for Signal Processing	SC	4	1	0	5

Prerequisites:

1. Concepts of DSP systems and its architecture.
2. Basic knowledge on FIR digital filters.
3. Concepts of retiming and systolic architecture.
4. Knowledge of recursive and adaptive filters.
5. Basics on algorithms used in fast convolution method.

Course Objectives:

1. To understand the basic concepts of DSP algorithms.
2. To analyze the various pipelining and parallel processing techniques.
3. To analyze the retiming and unfolding algorithms for various DSP applications.

Course Outcomes:

On completion of this course the student will be able to:

1. Apply DSP algorithms on to the IC technology
2. Analyze the concept of pipelining and other processing for DSP applications

Mapping of Course Outcomes with programme Outcomes

Course Code	POS/ COs	PO1	P02	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
M18VP3022	CO1	1		2			3							3	1	2
	CO2	1	3				3							2	1	3

Course Contents:

Unit 1: Introduction to DSP systems

Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.

Iteration Bounds:Data flow graph Representations, loop bound and Iteration bound, Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

Pipelining and parallel processing, pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

Unit 2: Retiming

Definition and Properties, Solving Systems of Inequalities, Retiming Techniques, Unfolding an Algorithm for Unfolding, Properties of Unfolding, and Critical path, Unfolding and Retiming, Application of Unfolding.

Systolic architecture design:systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays**.**

Unit 3:Fast convolution

Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic Convolution Design of fast convolution Algorithmby Inspection.

Unit 4: Pipelined and Parallel recursive and adaptive filter

Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using

Pipe lining and parallel processing, pipelined Adaptive digital filter.

References:

1. KeshabK.Parthi, "**VLSI Digital Signal Processing systems, Design and Implementation**", Wiley, Inter Science, 1999.
2. Mohammed Isamail and Terri Fiez, "**Analog VLSI Signal and Information Processing**", McGraw-Hill, 1994.
3. S.Y. Kung, H.J. White House, T. Kailath, "**VLSI and Modern Signal Processing**", Prentice Hall, 1985.
4. Jose E. France, YannisTsividis, "**Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing**", Prentice Hall, 1994.

Course Code	Course Title	Course Type	L	T	P	C
M18VP3031	High Speed VLSI Design	SC	4	1	0	5

Prerequisites:

1. Knowledge on high speed digital design and its issues.
2. Concept of noise and power supply network.
3. Principles of synchronization and timing convention.
4. Basic knowledge on clocked and no clocked logics and latching strategies.

Course Objectives:

1. Introduce the concept of high speed digital circuits.
2. Understand the power distribution and noise sources in VLSI circuits.
3. Understand the importance of timing analysis in high speed VLSI circuits.
4. Introduce the concept of latch and clock driven logic circuits for high speed VLSI circuits.

Course Outcomes:

On completion of this course the student will be able to:

1. Identify and analyse the sources of noise in VLSI circuits.
2. Describe the Signalling modes for transmission lines in VLSI circuits
3. Perform the timing analysis for VLSI Circuits
4. Design the clocked and non-clocked logic circuit
5. Design various latch based digital circuits.

Mapping of Course Outcomes with Program Outcomes:

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
M18VP3031	**CO1**	**3**	**3**							**3**	**3**	**2**				
	CO2	**3**	**2**	**3**						**3**	**3**	**3**		**3**		**3**
	CO3	**3**	**3**							**3**	**2**	**3**				
	CO4	**3**	**3**							**2**	**1**	**3**		**3**		
	CO5	**3**	**3**							**2**	**1**	**3**		**3**		

Course Contents:

Unit 1: Introduction to High Speed Digital Design

Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power.Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

Unit 2: Power distribution and Noise

Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference.

Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

Unit 3: Timing Convention and Synchronization

Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock distribution, clock skew and methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DLL based clock aligners.

Unit 4: Clocked & Non-Clocked Logics

Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass GateLogic, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

Latching Strategies:Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

Reference Books:

1. William S. Dally & John W. Poulton, "**Digital Systems Engineering**", *Cambridge University Press*, 1998.
2. Kerry Bernstein &ET. Al., "**High Speed CMOS Design Styles**", Kluwer, 1999.
3. Howard Johnson & Martin Graham, "**High Speed Digital Design**" A Handbook of Black Magic, *Prentice Hall PTR*, 1993.
4. Masakazu Shoji, "**High Speed Digital Circuits**", *Addison Wesley Publishing Company*, 1996.
5. Jan M, Rabaey, et al, "**Digital Integrated Circuits**", A Design Perspective, *Pearson*, 2003.

Course Code	Course Title	Course Type	L	T	P	C
M18VP3032	ASIC Design and Verification using SystemVerilog	**SC**	**4**	**1**	**0**	**5**

Prerequisites:

1. Fundaments knowledge of Digital System Design with Verilog HDL
2. Data Structures & Algorithm in C++

Course Objectives:

1. To study the basic concepts of systemverilog.
2. Study the different kinds of data types
3. Differentiate between HDL and HVL
4. Study the basic concepts of OOPs

Course Outcomes:

On completion of this course the student will be able to:

1. Model a scenario for Verification of a DUT in System Verilog
2. Analyze the usefulness of a driver, monitor, checker, test cases in a verification environment
3. Understand different kinds of datatypes and can distinguish difference between an HDL and HVL
4. Design test bench to verify the functionality of a design
5. Understand the concept of randomization and its importance in verification coverage in a bigger design
6. Able to design a VIP for an IP as a project

Mapping of Course Outcomes with Program Outcomes:

Course Code	POS/ COs	PO1	P02	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO1	PSO2	PSO3
M18VP3032	**CO1**	**3**	**2**	**2**	**3**	**3**	**3**		**3**	**2**	**2**	**1**	**3**	**3**	**3**
	CO2	**3**	**2**	**2**	**3**	**3**	**3**		**3**	**2**	**2**	**1**	**3**	**3**	**3**
	CO3	**3**	**3**	**2**	**3**	**3**	**3**		**3**	**2**	**2**	**1**	**3**	**3**	**3**
	CO4	**3**	**2**	**2**	**2**	**2**	**3**		**3**	**2**	**2**	**1**	**2**	**2**	**2**
	CO5	**3**	**2**	**2**	**3**	**3**	**3**		**3**	**2**	**2**	**1**	**3**	**3**	**3**
	CO6	**3**	**2**	**2**	**3**	**3**	**3**		**3**	**2**	**2**	**1**	**3**	**3**	**3**

Course Contents:

Unit 1: Verification Guidelines and Data Types

Introduction, The Verification Process, The Verification Plan, The Verification Methodology, Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench, Building a

Layered Testbench, Simulation Environment Phases, Maximum Code Reuse, Testbench Performance. Introduction to data types, Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Expression Width, Net Types.

Unit 2: Procedural Statements and Routines

Introduction, Procedural Statements, Tasks, Functions, and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

Unit 3: Basic OOPs

Introduction, Think of Nouns, not Verbs, Your First Class, Where to Define a Class, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects, Public vs. Private Straying Off Course, Building a Testbench.

Unit 4:Connecting the Testbench and Design

Introduction, Separating the Testbench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, Connecting It All Together, Top-Level Scope, Program – Module Interactions, SystemVerilog Assertions, The Four-Port ATM Router.

Current Trends in Testing and Verification: Advanced verification methodologies, e.g., UVM and OVM at basic levels. Cadence-IUS / Mentor-QuestaSim EDA Development Environment.

References:

1. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Publisher:Springer-Verlag New York, Inc. Secaucus, NJ, USA, 2006

2. Donald Thomas, Logic Design and Verification Using SystemVerilog, CreateSpace Independent Publishing Platform, 2014.

3. Language Reference Manual for SystemVerilog.

Semester – IV:

Course Code	Course Title	Course Type	L	T	P	C
M18VP4011	MSP430	SC	4	0	1	5

Prerequisites:

1. Knowledge on basics of MSP430 architecture.
2. Concepts of Interrupts and Interfacing techniques in MSP430.
3. Basic knowledge of I^2C and serial communication.
4. Practical knowledge on MSP430 programming.

Course Objectives:

1. Study the introduction to the TI MSP430 family of microcontrollers, their architecture, peripheral features and programming.
2. Understand and Provide theoretical and practical aspects of low-power system development using the MSP430.
3. Know the peripheral features of the MSP430, which include timers, digital and analog IO and serial communication modules.
4. Understand and Present case studies of application of the MSP430 so that the student can handle embedded system design projects independently.
5. Know the applications of the MSP430 in embedded systems.

Course Outcomes:

On completion of this course the students will be able to:

1. Design, develop, and evaluate software or a software/hardware system, component, or process to meet desired needs within realistic constraints.
2. Demonstrate and function on multi-disciplinary teams working in mechatronics and low power embedded systems.
3. Design, identify, formulate, and solve engineering problems
4. Analyse the need for, and an ability to engage in life-long learning and continuing professional development
5. Analyse a problem, and identify and define the computing requirements appropriate to its solution.
6. Design and develop principles in the construction of software systems of varying complexity.

Mapping of Course Outcomes with Program Outcomes

Course Code	POS/ COs	PO 1	P 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
M18VP4011	**CO1**	**3**	**1**	**1**	**1**			**3**					**3**	**3**	**2**	**2**
	CO2	**2**	**1**	**2**	**1**			**3**					**3**	**3**	**2**	**1**
	CO3	**2**	**1**	**2**				**3**					**3**	**3**	**2**	**2**
	CO4			**3**				**3**					**3**			**2**
	CO5	**2**	**1**	**2**				**3**					**3**	**3**	**2**	**2**
	CO6	**2**	**1**	**2**				**3**					**3**	**3**	**2**	**2**

Course Contents:

Unit 1:MSP430 Architecture and Programming

Architecture of the MSP430, addressing modes, instruction set, development environment, MSP430 programming in C and assembly language.

Unit 2:Interrupts and Digital IO in the MSP430

Interrupts, interrupt service routines, low-power modes of operation, parallel ports, digital inputs, and outputs, driving heavier loads, liquid crystal displays, driving an LCD from an MSP430x4xx.

Unit 3:Timers and Analog IO in the MSP430

Watchdog timer, basic timer1, timer_A, measurement in the capture mode, pulse-width modulation, modes of timer_A and timer_B, comparator_A, basic operation of the ADC10 and ADC12, the SD16_a sigma–delta ADC.

Unit 4:Communication Peripherals the MSP430

SPI and I²C features in MSP430, asynchronous serial communication, case studies of the applications of the MSP430 in embedded systems.

References:

1. John Davies, "**MSP430 Microcontroller Basics**", Newnes (Elsevier Science), 2008.
2. C P Ravikumar, "**MSP430 Microcontroller in Embedded System Project**," Elite Publishing House Pvt. Ltd., December 2011.
3. **MSP430 Teaching CD-ROM**, Texas Instruments, 2008.
4. Sample Programs for MSP430 downloadable from *www.msp430.com.*

Course Code	Course Title	Course Type	L	T	P	C
M18VP4012	FPGA Based Embedded System Design	SC	4	0	1	5

Prerequisites:

Concepts of digital system design and behavior modelling of a system, Basics of Verilog and VHDL, Knowledge of sequential and combinational circuits.

Course Objectives:

This course will enable students to:

1. Know FPGA architecture, interconnect and technologies.
2. Analyze the FPGA architecture and design implementation methodologies.
3. Explore the configuration, implementation and testing of embedded system on FPGA.

Course Outcomes

After completion of the course a student will be able to:

1. Design the reconfigurable digital systems.
2. Demonstrate and Debug the embedded systems before the actual product is developed.
3. Design finite state machines for various applications.
4. Implement, Design and develop embedded system using FPGA and EDA tools.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO 3
M18VP4012	**CO1**	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO2	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO3	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO4	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**

Course Contents:

Unit 1: Introduction **[14]**

Embedded System Overview, Hypothetical Robot Control System, Digital Design Platforms, Use of Pre-designed HDL Codes, Simulating Digital Logic Using Verilog

Unit 2: FPGA and CPLD

Architecture of a FPGA, FPGA Interconnect Technology, Logic Cell, FPGA Memory, Clock

Distribution and Scaling, Standards, Multipliers, Floor Plan and Routing, Timing Model for a FPGA, FPGA Power Usage

Unit 3: FPGA-based Embedded Processor

Hardware–Software Task Partitioning, FPGA Fabric Immersed Processors, Soft Processors, Hard Processors, Tool Flow for Hardware–Software Co-design, Interfacing Memory to the Processor, Interfacing Processor with Peripherals, Types of On-chip Interfaces, Wishbone Interface, Avalon Switch Matrix, OPB Bus Interface, Design Re-use Using On-chip Bus Interface, Creating a Customized Microcontroller, Robot Axis Position Control

Unit 4: FPGA-based Signal Interfacing and Conditioning

Serial Data Communication, Physical Layer for Serial Communication, RS-232-based Point-to-Point Communication, RS-485-based Multi-point Communication, Serial Peripheral Interface (SPI), Signal Conditioning with FPGAs, Prototyping Using FPGAs, Test Environment for the Robot Controller

Text Books:

1. Rahul Dubey, "**Introduction to Embedded System Design Using Field Programmable Gate Arrays**", Springer, 2008
2. Peter Ashenden, "**Digital Design using VHDL**", Elsevier, 2007.
3. Peter Ashenden, "**Digital Design using Verilog**", Elsevier, 2007.

Reference Books:

1. M.J.S. Smith, "**Application Specific Integrated Circuits**", Pearson, 2000.
2. W.Wolf, "**FPGA based system design**", Pearson, 2004.
3. Clive Maxfield, "**The Design Warriors's Guide to FPGAs**", Elsevier, 2004.

Course Code	Course Title	Course Type	L	T	P	C
M18VP4013	Synthesis and Optimization of Digital Circuits	SC	4	1	0	5

Prerequisites:

1. Basics of microelectronics, semiconductor technologies.
2. Concepts of system modeling and different optimizations of combinational logic circuit.
3. Knowledge on transformations, synthesis and delay calculation for combinational circuit.
4. Basics of scheduling algorithm.

Course Objectives:

1. To understand different methods used for the simplification of Boolean functions.
2. To understand and implement combinational, synchronous, and asynchronous sequential circuits.

3. To be acquainted with the MOS devices, system level design.
4. To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits using computer aided synthesis.
5. To provide hands on experience to the concepts taught in class.

Course Outcomes:

On completion of this course the students will be able to:

1. Design combinational and sequential circuits
2. Differentiate between Mealy and Moore model state machines, and draw a block diagram of each.
3. Describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P- channel MOSFETs and draw their circuit diagrams.
4. Define logic gate fan-in and describe the basis for its practical limit.
5. Calculate the DC noise immunity margin of a logic circuit and describe the consequence of an insufficient margin.
6. Design and demonstrate some basic projects based on sequential design.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO 3
M18VP 4013	CO1	3	3	3		2				2	3		3	2	3	2
	CO2	3	3			2				2	3		3	2	3	2
	CO3	3	3	3		2				2	3		3	2	3	2
	CO4	3	3	3		2				2	3		3	2	3	2
	CO5	3	3	3		2				2	3		3	2	3	2
	CO6	3	3	3		2				2	3		3	2	3	2

Course Contents

Unit 1: Introduction

Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Unit 2: Hardware Modeling

Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization:Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Unit 3: Multiple Level Combinational Optimizations

Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization. Sequential Circuit Optimization:Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Unit 4: Schedule Algorithms

A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding:Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

References:

1. Giovanni De Micheli, "**Synthesis and Optimization of Digital Circuits**", Tata McGraw-Hill, 2003.
2. ZviKohavi, "**Switching and Finite Automata Theory**", Tata McGraw Hill, thirdedition, 2000.
3. Alan B.Marcovitz, "**Intro. To Logic Design**", TMH, second edition, 2002.
4. SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, "**Logic Synthesis**", McGraw-Hill, USA, 1994.
5. Neil H.E. Weste and David money harris, "C**MOS VLSI Design: A circuits and system Perspective**",fourth edition, Pearson Education (Asia) Pvt. Ltd., 2000.
6. Kevin Skahill, "**VHDL for Programmable Logic**", Pearson Education (Asia) Pvt. Ltd., 2000.

Course Code	Course Title	Course Type	L	T	P	C
M18VP4014	CMOS RF Circuit Design	SC	4	1	0	5

Prerequisites:

1. Concepts of RF design and wireless technology.
2. Basic knowledge on RF modulation techniques.
3. Knowledge on behaviour and characteristics of BJT and MOSFET.

Course Objectives:

1. Understanding of the design and analysis of radio frequency integrated circuits and systems (RFICs) for communication.
2. Integrated Electronic Circuit Design which covers transistor-level design.

Course Outcomes:

On completion of this course the student will be able to:

1. Describe and understand the general challenges in the design of CMOS RF circuits.
2. Design matching circuits using passive RLC components.
3. Use various techniques to design high-frequency amplifiers.
4. Design and analyze oscillators.
5. Understand fundamentals of phase noise in oscillators.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PSO1	PSO2	PSO3
M18VP4014	**CO1**	**3**	**3**	**3**	**3**								**2**	**3**	**3**
	CO2	**3**	**2**	**2**	**3**								**2**	**3**	**3**
	CO3	**4**	**2**	**3**	**2**	**4**							**2**	**3**	**3**
	CO4	**3**	**3**	**3**	**3**	**2**		**2**					**3**	**3**	**3**
	CO5	**3**	**3**	**3**	**3**	**2**		**2**					**3**	**3**	**3**

Course Contents:

Unit 1: Introduction to RF Design and Wireless Technology

Design and Applications, Complexity and Choice of Technology**.**

Basic concepts in RF design:Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion**.**

Unit 2: RF Modulation

Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, direct conversion and two-step transmitters.

Unit 3: BJT and MOSFET Behavior at RF Frequencies

BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation.

Unit 4: RF Circuits Design

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks.

Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range,various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures
And frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Reference Books:

1. B. Razavi, "**RF Microelectronics**" PHI 1998.
2. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
3. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
4. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996.

Course Code	Course Title	Course Type	L	T	P	C
M18VP4015	Advances in VLSI Design	SC	4	1	0	5

Prerequisites:

1. Concepts of MOS and CMOS circuits.
2. Knowledge on BICMOS, steering logic and buffers.
3. Differences between MOS and CMOS.
4. Concepts of various design methods in CMOS.

Course Objectives:

1. To understand the basics and operation of static, comparison between CMOS and BiCMOS.
2. To understand short channel effects.
3. To understand the challenges to CMOS.
4. To understand the super buffers, layouts and technology mapping.

Course Outcomes

On completion of this course the student will be able to:

1. Learn advanced technologies in the fields of VLSI design with the fundamental concepts.
2. Apply advanced technical knowledge in multiple contexts.
3. Understand and design advanced VLSI based system and analyse and interpret results.
4. Use the techniques, skills, modern Electronic Design

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	P02	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	P O 10	P O 11	P O 12	PS O 1	PS O 2	PS O 3
M18VP4015	**CO1**	**1**		**2**			**3**							**3**	**1**	**2**
	CO2		**1**	**2**			**3**							**2**	**1**	**3**
	CO3				**2**	**1**	**3**							**3**	**2**	**1**
	CO4		**2**	**1**	**3**											

Course Contents:

Unit 1: Review of MOS Circuits

MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS Miniaturization.

Unit 2: Beyond CMOS

Evolutionary advances beyond CMOS, carbon Nanotubes, conventional vs. tactile computing, computing, molecular and biological computing - molecular Diode and diode- diode logic. Defect tolerant computing.

Super Buffers, Bi-CMOS and Steering Logic:Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

Unit 3: Special Circuit Layouts and Technology Mapping

Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module layout.

Unit 4: System Design

CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach,

Full custom design.

Reference Books:

1. Kevin F Brennan "**Introduction to Semi-Conductor Device**", Cambridge publications, 2006.

2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications, 1990.

3. D.APucknell. "**Basic VLSI Design**", PHI Publication, 2005.

4. Wayne Wolf, "**Modern VLSI Design**" Pearson Education, Second Edition, 2002.

Course Code	Course Title	Course Type	L	T	P	C
M18VP4021	MEMS	SC	4	1	0	5

Prerequisites

Engineering Physics, Upper Division standing in Engineering, Chemistry or Chemical Engineering and Material Science, VLSI Technology, Elements of Mechanical Engineering.

Course Objectives:

This course will enable students to:

1. Introduce the basic three pillars of MEMS design, fabrication and materials.
2. To introduce different materials used for MEMS.
3. To provide knowledge of semiconductors and solid mechanics to fabricate MEMS devices
4. Highlight the various electrical and mechanical concepts with regards to MEMS arena.
5. Demonstrate the various fabrication and micro machining techniques.
6. Recognize the basic operation principles Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties.
7. Understand Etch mechanism, reactive Plasma Etching techniques and Equipment.
8. To introduce various sensors and actuators.

Course Outcomes:

On completion of this course the student will be able to:

1. Differentiate between micro systems, MEMS and NEMS
2. Assess the various electro-mechanical properties of materials used for MEMS design
3. Describe the various steps involved in the MEMS fabrication
4. Analyze the chemical and physical vapor processes; heteroepitaxy and defects; substrates and substrate engineering
5. Convey knowledge of advanced concepts of lithography and etching
6. Explore electrostatic, thermal, piezoelectric and magnetic actuators at micro scale

Mapping of Course Outcomes with programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
	CO1	1		2		3		3					4	1		2
	CO2	1			2	3		4		3				1		2
	CO3	1	1	2		3	4	2						1		2
	CO4	1		3			2					3	4	1		2
M18VP4021	CO5	1		3			2					3	4	1		2
	CO6	1		3			2					3	4	1		2

Course Contents

Unit 1: Introduction to MEMS

Overview of MEMS and Microsystems: What are MEMS, Why Miniaturization, Why microfabrication, Microsystems versus MEMS, Smart Materials, Structures and Systems, Integrated Microsystems, Typical MEMS and Microsystem Products, The Multidisciplinary nature of Microsystem design and manufacture, Applications of smart Materials and Micro Systems, Applications of Aerospace, Biomedical and Automotive industry.

Materials for MEMS: Silicon compatible material System-Silicon, Czochralski Crystal Growing, Silicon oxide and Nitride, Thin metal Films, Polymers, Other material and substrates.

Unit 2: Microsystems Fabrication Process

Epitaxy: Introduction, Vapor-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation.

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, Some MEMS fabrication processes: surface micro-machining, bulk micromachining, LIGA process.

Unit3: Microsystems Design and Packaging

Assembly, Packaging, and Testing (APT) of Microsystems, Microsystem Packaging, overview of Mechanical Packaging of Microelectronics, interfaces in Microsystem Packaging, Essential Packaging Technologies, Three Dimensional Packaging, Assembly of Microsystems, Selection of Packaging Materials.

Unit 4: Micro Sensors, Actuators, Systems and Smart Materials

Case studies – silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conduct metric gas sensor, silicon micro-mirror arrays, piezo-electric based inkjet print head, electrostatic comb-drive and magnetic micro relay, portable clinical analyzer, active noise control in a helicopter cabin.

VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC technology, CMOS IC Technology, MOS Memory IC Technology, Bipolar IC Technology, IC Fabrication.

Text Books:

1. G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre, "**Micro and Smart Systems**", *Wiley India, 2010.*
2. Chang Liu, "**Foundation of MEMS***" Pearson Education International, 2006.*
3. Tai Ran Hsu, "**MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering**, *Wiley, 2008.*

Reference Books:

1. S. M. Sze,**"VLSI Technology",** *McGraw-Hill, Second Edition.*
2. NadimMaluf, Kirt Williams "**An Introduction to Microelectromechanical Systems Engineering"** Second addition.

Course Code	Course Title	Course Type	L	T	P	C
M18VP4022	Advanced Computer Architecture	SC	4	1	0	5

Prerequisites:

1. Concepts of computer design, pipelining and instruction level parallelism.
2. Knowledge on design of memory hierarchy and real faults in a system.
3. Basic knowledge on very long instruction word and EPIC.
4. Concepts of multiprocessors and interprocessor communication.
5. Concepts of computer arithmetic.

Course Objectives:

1. Introduce the fundamentals of computer design.
2. Understand the quantitative principles of computer design and their performance.
3. Understanding the concepts of instruction level parallelism.
4. Introduce the fundamentals of advanced memory hierarchy.
5. Introduce the basics of VLIW processors.
6. Understand the concepts of multiprocessors and inter process communication.
7. Study of computer arithmetic blocks.

Course outcomes:

On completion of this course the student will be able to:

1. Analyse the importance of power and performance for given computer architecture.
2. Identifying the pitfalls and fallacies for the performance in the computer architecture.
3. Describe the instruction level parallelism and its importance with respect to performance and power dissipation in computer architecture
4. Calculate the performance of I/O devices
5. Designing the efficient hardware and software for the VLIW processors.
6. Designing the efficient arithmetic components for computer architecture.

Mapping of Course Outcomes with Program Outcomes

Course Code	POS/ COs	PO 1	P 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
M18VP4022	**CO1**	**3**		**1**				**3**					**3**	**3**	**2**	**2**
	CO2	**2**		**2**				**3**					**3**	**3**	**2**	**1**
	CO3	**2**		**2**				**3**					**3**	**3**	**2**	**2**
	CO4			**3**				**3**					**3**			**2**
	CO5	**2**		**2**				**3**					**3**	**3**	**2**	**2**
	CO6	**2**		**2**				**3**					**3**	**3**	**2**	**2**

Course Contents:

Unit 1: Introduction and Review of Fundamentals of Computer Design

Introduction; Classes computers, Defining computer architecture, Trends in Technology, Trends in power in Integrated Circuits, Trends in cost, Dependability, Measuring, reporting and summarizing Performance, Quantitative Principles of computer design, Performance and Price-Performance; Fallacies and pitfalls; Case studies.

Some topics in Pipelining, Instruction –Level Parallelism, Its Exploitation and Limits on ILP:Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining, Basic concepts and challenges of ILP, Case study of Pentium 4, Fallacies and pitfalls.

Introduction to limits in ILP, Performance and efficiency in advanced multiple-issue processors.

Unit 2: Memory Hierarchy Design, Storage Systems

Review of basic concepts, Cross cutting issues in the design of memory hierarchies, Case study of AMD Opteron memory hierarchy, Fallacies and pitfalls in the design of memory hierarchies, Introduction to Storage Systems, Advanced topics in disk storage.

Definition and examples of real faults and failures: I/O performance, reliability measures, and benchmarks; Queuing theory; Crosscutting Issues, Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls.

Unit 3: Hardware and Software for VLIW and EPIC Introduction

Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism, Hardware Support for Exposing Parallelism: Predicated Instructions, Hardware Support for Compiler Speculation, The Intel IA-64 Architecture and Itanium Processor, Concluding Remarks.

Unit 4:Large-Scale Multiprocessors and Scientific Applications Introduction, Interprocessor Communication

The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory

Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications,

Implementing Cache Coherence, the Custom Cluster Approach: Blue Gene/L, Concluding Remarks.

Computer Arithmetic: Introduction, Basic Techniques of Integer Arithmetic, Floating Point, Floating-Point Multiplication, Floating-Point Addition, Division and Remainder, More on Floating-Point Arithmetic, Speeding Up Integer Addition, Speeding Up Integer Multiplication and Division, Fallacies and Pitfalls.

Reference Books:

1. Hennessey and Patterson, "**Computer Architecture A Quantitative Approach**", 4th Edition, Elsevier, 2007.
2. Kai Hwang, "**Advanced Computer Architecture - Parallelism, Scalability, Programmability**", 2nd Edition, 1992.

Course Code	Course Title	Course Type	L	T	P	C
M18VP5040	**Automotive Electronics System**	**OE**	**3**	**1**	**0**	**4**

Course Objectives:

1. Understand the functions of electronic systems in modern automobiles, modern electronics technology to improve the performance, safety, comfort and related issues
2. Study the principles of automotive sensors and interfacing techniques, design, model and simulate interfacing systems with sensors
3. Know the principles and functionalities of various Automotive Communication Protocols (ACPs), Design ACP based In-Vehicle Networks(IVNs), selection of ACPs for various application in Automotive
4. Know the industry standard practices for ECU design for automotive, modeling and analysis of application software for ECU design and development, design of ECUs for automobiles, design of HIL and fault diagnostics

Course Outcomes:

On completion of the course the students will be able to:

1. Implement and Interface sensors and for various automotive applications
2. Design and diagnose the faults in the systems Implement automotive fault diagnostics and faults
3. Analyze on and off board diagnostics, diagnostics protocol.

Mapping of Course Outcomes with Program Outcomes

Course Code	POs/ COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO 1	PSO 2	PSO 3
M18VP5040	CO1	2	1					2				3	1		2
	CO2	1	2	1		3			3				1		2
	CO3	1		1			2				3		1		2

Course Contents:

Unit 1: Automotive Industry and Modern Automotive Systems [14]

Vehicle classifications and specifications, need for electronics in automobiles, Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Spark and Compression Ignition Engines, Ignition systems, Spark plug, Spark pulse generation, Ignition Timing. Transmission Control - Automotive transmissions, Drive Train, Brakes, Steering System - Steering Control, Starting System- Battery, Air/Fuel Systems, Fuel Handling, Air Intake System, Lighting.

Unit 2: Introduction to Automotive Sensors and Instrumentation [14]

Sensors and actuators, Air/ Fuel Management Sensors – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor Sensors in Engine control, adaptive cruise control, braking control, traction control, steering, stability, Lighting, wipers, climate control, Sensors for occupant safety, Sensor and actuator interfacing techniques and electronic displays. Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Unit 3: Control Systems [14]

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control Communication – Serial Data, Communication Systems, Power windows, Remote keyless entry systems, GPS,Automotive Communication Protocols Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, Vehicle Motion Control – Cruise Control, Chassis, , Power Brakes, antilock braking systems, Electronic stability and other technologies, Traction Control, Electronic Stability Control, Electronically controlled suspension Fundamentals of electronically controlled steering system, Power Steering,

Unit 4: Safety and Convenience [14]

Electronics for Passenger Safety and Convenience – SIR, Air bag and seat belt pretension systems, Tire pressure monitoring systems, Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters Integrated Body – Climate Control Systems, Electronic HVAC Systems, Lighting, Entertainment Systems Automotive Diagnostics – Timing Light, Engine Analyzer, Process of Automotive Fault Diagnostics, Fault Codes, On-board diagnostics, Off-board diagnostics, Expert Systems. Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System, AFS.

Reference Books:

1. Denton. Burlington "**Automotive Electrical and Electronic Systems**", MA 01803, Elsevier Butterworth-Heinemann, 2004.
2. Ronald K. Jurgen. "**Automotive Electronics Handbook**", 2nd Edition, McGraw-Hill, 2007
3. Christian Kohler, "**Enhancing Embedded Systems Simulation**" Vieweg+TeubnerVerlag/ Springer, 2011.
4. Gabriela Nicolescu and Pieter J. Mosterman, "**Model-Based Design for Embedded Systems**", CRC Press, 2010
5. Gilbert Held, "**Inter- and Intra-Vehicle Communications**", CRC Press, 2007.
6. William B. Ribbens, "**Understanding Automotive Electronics**", 5th Edition, Newnes, 2006
7. Bosch, "**Automotive Electrics & Electronics**", Robert Bosch GmbH, 3rd Edition, 1999.

CAREER DEVELOPMENT AND PLACEMENT

Having a degree will open doors to the world of opportunities for you. But Employers are looking for much more than just a degree. They want graduates who stand out from the crowd and exhibit real life skills that can be applied to their organizations. Examples of such popular skills employers look for include:

- Willingness to learn
- Self motivation
- Team work
- Communication skills and application of these skills to real scenarios
- Requirement of gathering, design and analysis, development and testing skills
- Analytical and Technical skills
- Computer skills
- Internet searching skills
- Information consolidation and presentation skills
- Role play
- Group discussion, and so on

REVA University therefore, has given utmost importance to develop these skills through variety of training programs and such other activities that induce the said skills among all students. A full-fledged Career Counseling and Placement division, namely Career Development Center (CDC) headed by well experienced senior Professor and Dean and supported by dynamic trainers, counselors and placement officers and other efficient supportive team does handle all aspects of Internships and placements for the students of REVA University. The prime objective of the CDC is to liaison between REVA graduating students and industries by providing a common platform where the prospective employer companies can identify suitable candidates for placement in their respective organization. The CDC organizes pre-placement training by professionals and also arranges expert talks to our students. It facilitates students to career guidance and improve their employability. In addition, CDC forms teams to perform mock interviews. It makes you to enjoy working with such teams and learn many things apart from working together in a team. It also makes you to participate in various student clubs which helps in developing team culture, variety of job skills and overall personality.

The need of the hour in the field of Electronics and Communication Engineering is efficient leaders of repute, who can deal the real time problems with a flavour of innovation. This kept in focus, the CDC has designed the training process, which will commence from second semester along with the curriculum. Special coaching in personality development, career building, English proficiency, reasoning, puzzles, leadership, and strategic management and communication skills to every student of REVA University is given with utmost care. The process involves continuous training and monitoring the students to develop

their soft skills including interpersonal skills that will fetch them a job of repute in the area of his / her interest and march forward to make better career. The School of Electronics and Communication Engineering also has emphasised subject based skill training through lab practice, internship, project work, industry interaction and many such skilling techniques. The students during their day to day studies are made to practice these skill techniques as these are inbuilt in the course curriculum. Concerned teachers also continuously guide and monitor the progress of students.

The University has recognized skill development and industry relationship as its very important activities. Therefore, the University-Industry Interaction and Skill Development Centre headed by a Senior Professor & Director has been established to facilitate skill related training to REVA students and other unemployed students around REVA campus. The center conducts variety of skill development programs to students to suite to their career opportunities. Through this skill development centre the students shall compulsorily complete at least two skill / certification based programs before the completion of their degree. The University has collaborations with Industries, Corporate training organizations, research institutions and Government agencies like NSDC (National Skill Development Corporation) to conduct certification programs. REVA University has been recognised as a Centre of Skill Development and Training by NSDC (National Skill Development Corporation) under PradhanMantriKaushalVikasYojana.

The various skill/certification programs identified are as follows:

- Big-data and Cloud Computing, Internet of Things (IOT), Xilinx, NS-2, Cadence, ANSYS, Advanced C C++ and Internals of LINUX/UNIX
- Red-Hat certified programs on LINUX
- Management related programs like SAP, ERP and Business Analytics.
- Open Source software/hardware, Software Testing
- Advanced networking based CISCO / Microsoft technology.
- Web designing, System administration,
- IBM certified programs.

The University has signed MOU's with Multi-National Companies, research institutions, and universities abroad to facilitate greater opportunities of employability, students' exchange programs for higher learning and for conducting certification programs.

Rukmini Knowledge Park
Kattigenahalli, Yelahanka,
Bengaluru – 560064, INDIA

Tel : +91 80 46966966
Fax : +91 80 4696 6998

www.reva.edu.in